ADRET

SYNTHÉTISEUR DE FRÉQUENCE
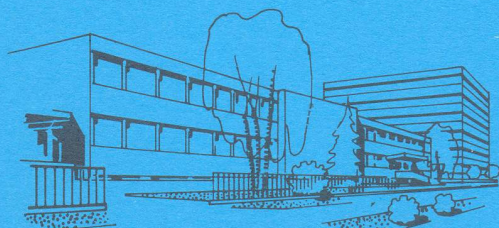## *FREQUENCY SYNTHESIZER*
0,01 Hz / 200 kHz

3100 B

ADRET

SYNTHÉTISEUR DE FRÉQUENCE
FREQUENCY SYNTHESIZER

0,01 Hz/200 kHz

3100 B

ERRATA No 1

Date ___ JULY 12TH, 1979 _____

Valid from serial No _13 _____

Date of delivery _____

CONCERNS INSTRUCTIONS MANUAL FOR _ 3100B AND OPTIONS _____

Edition _ 2ND _____

Page or plate	INSTEAD OF	READ
PLATE VI-7	Q3 : 2N 2219 Q6 : 2N 2905 Q7 : 2N 2219 Q12 : 2N 2905 CR5, CR6, CR11 and CR12 : 1N 4448	Q3 : BD 135 Q6 : BD 136 Q7 : BD 135 Q12 : BD 136 Transistors BC 184C whose collector and base are short-circuited.
PLATE VI-18	Q15 : 2N 2219 Q16 : 2N 2905 CR9 : 1N 4448 CR10 : 1N 4448	Q15 : BD 135 Q16 : BD 136 Transistors BC 184C whose collector and base are short-circuited.

SUMMARY

LIST OF PLATES

I FUNCTIONAL DESCRIPTION

The 3100B ADRET synthesizer is a digitally controlled signal generator which delivers all 0.01 Hz to 200 kHz frequencies with 0.01 Hz resolution.

The synthesized frequency can be either manually dialled through eight rotary switches on the front panel of the instrument (Local mode), or programmed in parallel BCD code through TTL signals sent to the programming connector on the rear panel of the instrument (Remote mode).

Two channels A and B simultaneously deliver two output signals in phase quadrature with 5 Ω or 50 Ω impedance and an electromotive force adjustable from 0 to 10 Vpeak. Moreover, the signal delivered by channel A can have the following forms : sine wave, positive square wave, symmetrical square wave, negative square wave, TTL level square wave.

According to the user's needs, the 3100B generator synthesizer can be fitted with the following options :

- Option 3111B : programmable attenuator

This option allows to attenuate one of the output signals of the generator synthesizer from 0 dB to 79.9 dB with 0.1 dB resolution. The attenuation value can be either manually dialled through three rotary switches in Local mode, or programmed in parallel BCD code through TTL signals in Remote mode.

- Option 3112B : programmable phase-shifter

This option delivers a sinusoidal signal phase-shifted from 0° to 359.9° with regard to the signal of channel A of the 3100B generator synthesizer. The phase-shift value can be either manually dialled through four thumbwheel switches in Local mode, or programmed in parallel BCD code through TTL signals in Remote mode. The electromotive force of the phase-shifted signal is adjustable from 0 to 10 Vpeak with 5 Ω or 50 Ω output impedance.

- Option 3114B : Search and Sweep

This option allows progressive frequency variation of the generator synthesizer output signals. Four modes of operation are possible depending on the function required :

- Search function

- Free-run Sweep

- Triggered Sweep

- Search or Sweep by external signal

In all cases, twenty-one "birdy" or rectified markers display the frequency variation achieved.

II SPECIFICATIONS

II-1 SPECIFICATIONS OF SYNTHESIZER 3100B

FREQUENCY

Range : 0.01 Hz to 199 999.99 Hz

Resolution : 0.01 Hz

Selection : with 8 digits

Stability : $\pm$ 2.10^{-5} from 0°C to + 50°C

$\pm$ 5.10^{-7} per day after 8 hours'operation.

EXTERNAL REFERENCE

Substitution of the built-in master oscillator for the external reference.

Frequency : 10 MHz

Level : 50 mVrms to 1 Vrms/50 Ω.

10 MHz REFERENCE OUTPUT

Level : 100 mVrms/50 Ω.

OUTPUT SIGNALS

The synthesized signal is simultaneously available on four different outputs :

Main output A : Provides sine wave, positive , negative , symmetrical or
TTL square wave.

Main output B : Sine wave, phase-shifted from + 90° with respect to the outputs A wave.

Auxiliary output A : sine wave.

Auxiliary output B : sine wave, phase-shifted from + 90° with respect to the outputs A wave.

MAIN OUTPUT A

Provides sine wave, positive, negative, symmetrical or TTL square wave.

● Square waves rise and fall time : 100 ns

● Square waves duty cycle : 50 % $\pm$ 2 %

Output level :

● Sine wave :
  e.m.f. variable : 0 V to 10 V peak
  e.m.f. calibrated : 7 V peak $\pm$ 5 %

● Positive or negative square wave :
  e.m.f. variable : 0 V to 10 Vp-p
  e.m.f. calibrated : 7 Vp-p $\pm$ 5 %

● Symmetrical square wave :
  e.m.f. variable   : 0 V to 10 V peak
  e.m.f. calibrated : 7 V peak ± 5 %

● TTL square waves :
  e.m.f. calibrated : 3.8 V p-p ± 5 %

Output level flatness : ± 3 % within the entire frequency range.

Output impedance : 50 Ω or 5 Ω

Output current : maximum 100 mA peak

Output level attenuation (50 Ω impedance) :
● Dynamic range : 70 dB
● Resolution   : 10 dB
● Accuracy   : ± 0.5 dB

MAIN OUTPUT B

Sine wave with 90° phase-shift from main output signal.

Phase-shift accuracy with respect to main output sine wave with calibrated e.m.f. : ± 0.5°

Output level :
● e.m.f. variable   : 0 V to 10 V peak
● e.m.f. calibrated : 7 V peak ± 5 %

Output level flatness : ± 3 % within the entire frequency range.

Output impedance : 50 Ω or 5 Ω

Output current : maximum 100 mA peak

AUXILIARY OUTPUT A

Sine wave in phase with main output A.

Output level : 2 Vpeak e.m.f.

Load impedance : 1 kΩ minimum

AUXILIARY OUTPUT B

Sine wave with 90° phase-shift from signal of auxiliary output A.

Output level : 2 Vpeak e.m.f.

Load impedance : 1 kΩ minimum

SPECTRAL PURITY

(measured on main outputs with calibrated e.m.f. and 50 Ω impedance)

Sine wave harmonic signals : - 50 dB

Non-harmonic signals : - 70 dB

Phase noise in a 1 Hz band :
    - 110 dB at 100 Hz from carrier
    - 115 dB at 1 kHz from carrier
    - 125 dB at 10 kHz from carrier.

FREQUENCY PROGRAMMING

Selection of the Local or Remote mode is achieved either through a front-panel switch or through a rear-panel programming connector, with priority for the Remote mode.

- Current-source positive TTL logic :
    "1" level : + 2 V to + 5 V/0.1 mA
    "0" level : 0 V to + 0.4 V/0.2 mA

- 1-2-4-8 parallel BCD code

- Resolution : 0.01 Hz

- Settling times :

Digits affected by frequency switching	Settling time at 100 Hz from final frequency	Settling time at 10 Hz from final frequency
10^5 Hz to 10^3 Hz	0.5 ms	1 ms
Less than or equal to 10^2 Hz	Frequency error less than 1 Hz after 1 ms	

The above-mentioned settling times depend only on the weight of the digits affected by frequency switching.

POWER REQUIREMENTS

Voltage :   115 V/230 V ($\pm$ 10 %)

Frequency   :   50 Hz to 400 Hz

Consumption :   40 VA

MECHANICAL DATA

Adaptable to 19" rack

Height : 132 mm (3U)

Width   : 440 mm

Overall depth : 452 mm

Weight : 10 kg to 12 kg according to options.

TEMPERATURE RANGE

Operation : 0°C to + 50°C

Storage   : - 20°C to + 70°C

ATTENUATION

Dynamic range : 79.9 dB

Resolution   : 0.1 dB

Selection   : by 3 rotary switches

Characteristic impedance : 50 Ω

Accuracy :

- 0.1 dB steps : ± 0.05 dB
- 1 dB steps   : ± 0.1 dB
- 10 dB steps : ± 0.2 dB
- Maximum error : ± 1 dB

MAXIMUM PHASE-SHIFT
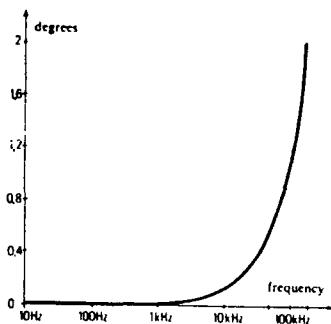
PROGRAMMING

- • Current-source positive TTL logic :
    "1" level : + 2 V to + 5 V/0.1 mA
    "0" level : 0 V to + 0.4 V/ 0.2 mA

- 1-2-4-8 parallel BCD code

- Resolution : 0.1 dB

- Switching time : 3 ms

II-3   SPECIFICATIONS OF OPTION 3112B

PHASE-SHIFT

Range : 0° to 359.9°

Resolution : 0.1°

Selection : by 4 thumbwheel switches

Phase-shift accuracy : measured with respect to the main output A sine wave, with calibrated e.m.f. and 50 Ω impedance.

● Linearity : $\pm$ 1°

● Phase/frequency response : $\pm$ 1°

● Phase/temperature response : $\pm$ 0.025 degree/°C

OUTPUT LEVEL

Waveform : sine wave

Output level :

● e.m.f. variable   : 0 V to 10 Vpeak

● e.m.f. calibrated : 7 V peak $\pm$ 5 %

Output level flatness : $\pm$ 3 % within the entire frequency range

Output impedance : 50 Ω or 5 Ω

Output current : maximum 100 mA peak

SPECTRAL PURITY

(measured with calibrated e.m.f. and 50 Ω impedance)

Harmonic signals :   - 45 dB

Non-harmonic signals :   - 65 dB

Phase-noise in a 1 Hz band :
- 110 dB at 100 Hz from carrier
- 115 dB at 1 kHz from carrier

PHASE-SHIFT PROGRAMMING

● Current-source positive TTL logic :
   "1" level : + 2 V to + 5 V/0.1 mA
   "0" level : 0 V to + 0.4 V/ 0.2 mA

● 1-2-4-8 parallel BCD code

● Resolution : 0.1°

● Switching time : 20 ms

OPERATING MODES

Manual mode : Continuous adjustment of the Synthesizer output frequency (Search function).

Free-run mode : Sweep by symmetrical triangular wave.

Triggered mode : Sawtooth sweep.

External mode : Sweep by external voltage.

MANUAL MODE (Search function)

Ranges : $\pm$ 1 Hz, $\pm$ 10 Hz, $\pm$ 100 Hz, $\pm$ 1 kHz, $\pm$ 10 kHz.

- Search range display by LED indicators on the 3100B Mainframe.

- Continuous adjustment by ten-turn potentiometer of the Synthesizer output frequency around the frequency set on the switches located on the left of Search range indicator.

- Frequency interpolation display on + 1, 0, - 1 graduated scale.
  Resolution : $\pm$ 2 %

Interpolation oscillator output :

On rear-panel BNC connector : 5 MHz $\pm$ 1 MHz for $\pm$ 100 % of the Search range.

- Level : approximately 200 mVrms/50 Ω

- Interpolation oscillator centering by front-panel split-shaft potentiometer.

- Stability : $\pm$ 10^{-3}/10 mn

FREE-RUN OR TRIGGERED MODE

Ranges : $\pm$ 1 Hz, $\pm$ 10 Hz, $\pm$ 100 Hz, $\pm$ 1 kHz, $\pm$ 10 kHz.

- Dispersion range display by LED indicators on the 3100B Mainframe.

- Continuous dispersion adjustment by ten-turn potentiometer, with display on + 1, 0, - 1 graduated scale.
  Resolution : $\pm$ 2 %

Interpolation oscillator output :

On rear-panel BNC connector : 5 MHz $\pm$ 1 MHz for $\pm$ 100 % of the dispersion range.

- Level : approximately 200 mVrms/50 Ω

- Interpolation oscillator centering by front-panel split-shaft potentiometer.

- Stability : $\pm$ 10^{-3}/10 mn

Sweep

- Duration : 10 ms to 300 s

- In triggered mode, Start/Stop controls by pushbutton on front-panel or "0" passing level on rear-panel.

- Sweep signal output :
  Amplitude   : $\pm$ 5 V
  Minimal load : 1 kΩ

EXTERNAL MODE

Ranges : $\pm$ 1 Hz, $\pm$ 10 Hz, $\pm$ 100 Hz, $\pm$ 1 kHz, $\pm$ 10 kHz.

● Dispersion range display by LED indicators on the 3100B Mainframe.
● Continuous dispersion adjustment by potentiometer within the selected dispersion range.

Sweep input

● 0.5 dB bandwidth : DC to 1 kHz
● Input impedance : 10 kΩ
● Sensitivity : $\pm$ 5 V for the entire dispersion range
● Linearity :
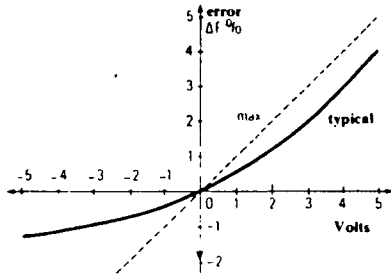
```
5 ┤ error
  │ Δf %
4 ┤
3 ┤
2 ┤   max        typical
1 ┤
  └─┬──┬──┬──┬──┬──┬──┬──┬──┬──┬──
 -5 -4 -3 -2 -1  0  1  2  3  4  5
                           Volts
 -1
 -2
```

Interpolation oscillator output :
    On rear-panel BNC connector : 5 MHz $\pm$ 1 MHz for $\pm$ 100 % of the dispersion range.

● Level : approximately 200 mVrms/50 Ω
● Interpolation oscillator calibration by front-panel split-shaft potentiometer
● Stability : $\pm$ 10^{-3}/10 mn

MARKERS

In Free-run or Triggered mode, as well as in External mode, two types of markers are available .

"BIRDY" MARKERS :

● Three markers indicating the center frequency and the extreme frequencies of the dispersion range.
   Amplitude : about 500 mVp-p/50 Ω
● 18 intermediate markers
   Amplitude : about 100 mVp-p/50 Ω
● Space between two markers : 10 % of the dispersion range

RECTIFIED MARKERS :

● 3 markers indicating the center frequency and the extreme frequencies the dispersion range.
   Amplitude : about 500 mV peak
● 18 intermediate markers
   Amplitude : about 100 mV peak
● Space between two markers :
   10 % of the dispersion range

● Minimal load : 1 kΩ

III PRINCIPLE OF OPERATION

III-1 GENERATOR SYNTHESIZER 3100B

The operation of the 3100B ADRET generator synthesizer is based on indirect frequency synthesis, which uses the phase-locking of an oscillator to a reference frequency by means of a programmable division rate counter.

The elaboration of the synthesizer output frequency is iteratively achieved through six subassemblies, as shown in the block-diagram of plate III-1.

- The Centade elaborates the 10^{-2} Hz and 10^{-1} Hz increments of the output frequency ;

- Four Standard Decades successively generate the 10^0 Hz, 10^1 Hz and 10^3 Hz increments of the output frequency ;

- The Twenty-Increment unit elaborates the ten 10^4 Hz increments and the two 10^5 Hz increments of the output frequency.

The frequency increments generated in each subassembly are incorporated in the following subassembly where they are divided by 10.

Thus, the Centade delivers a F1 frequency variable from 2 MHz to 1.901 MHz in 1 kHz and 10 kHz steps representing the 10^{-2} Hz and 10^{-1} Hz increments of the output frequency. This F1 frequency is sent to the first Standard Decade where it is added to the frequency carrying the 10^0 Hz increments of the output frequency and afterwards divided by 10.

This process provides a F2 frequency variable from 2 MHz to 1.9001 MHz in 100 Hz, 1 kHz and 10 kHz steps representing respectively the 10^{-2} Hz, 10^{-1} Hz and 10^0 Hz increments of the output frequency of the generator synthesizer.

The same method of operation is used in the other three Standard Decades and in the Twenty-Increment unit as well, where frequency F6 variable from 8 MHz to 7.200 000 04 MHz in 0.04 Hz steps is issued from, carrying all the increments of the output frequency.

This frequency F6 is divided by 4 in the Output Mixer through a counter providing two signals in phase quadrature. Two substractive mixing circuits receiving frequency F11 : 2 MHz issued from the Time Base serve to obtain two signals in phase quadrature, the frequency of which varies from 0.01 Hz to 199.999 99 kHz in 0.01 Hz steps. After amplification and shaping (channel A), these signals constitute the A and B outputs of the generator synthesizer.

III-2 OPTION 3111B

The 3111B programmable attenuator consists of ten attenuating cells controlled by a transcoder circuit which permits the parallel BCD programming.

III-3 OPTION 3112B

The generation of the sine wave phase-shifted from 0° to 359.9° which is delivered by the 3112B programmable phase-shifter is achieved by multiplying the sine waves issued from channels A and B of the Output Mixer by two DC voltages representing the cosine and the sine of the ϕ phase-shift angle, and then by adding the signals obtained according to the following formula :

$$\sin (\omega t + \phi) = \cos \phi . \sin \omega t + \sin \phi . \cos \omega t$$

The DC voltages representing cos ϕ and sin ϕ are elaborated through 3 kHz frequency TTL signals generated by a Digital Phase-Shift subassembly.

III-4 OPTION 3114B

The 3114B Search and Sweep option delivers a F12 frequency variable from 2.1 MHz to 1.9 MHz, which is substituted for one of frequencies F1 to F5, so as to permit continuous variation of the synthesizer output frequency within the selected interpolation range. The twenty-one markers spaced every 10 % of the interpolation range are generated by frequency beat between the interpolation oscillator frequency and a reference signal derived from the Time Base.

IV PRELIMINARY INSTRUCTIONS

IV-1 AC LINE CONNECTION

Connection to mains is achieved on socket (S03) through a three-prong standard cord supplied with the instrument.

Check that AC line voltage selector (K9) is on the position corresponding to the mains voltage, remembering that the 115 V and 230 V values admit $\pm$ 10 % variation.

Two (F1) and (F2) fuses of 250 mA each protect the instrument, without any need to change their value according to the mains voltage used.

In the case where the supply is by square-wave converter, the amplitude of these square waves must be 155 Vpeak and AC line voltage selector (K9) must be set on 115 V.
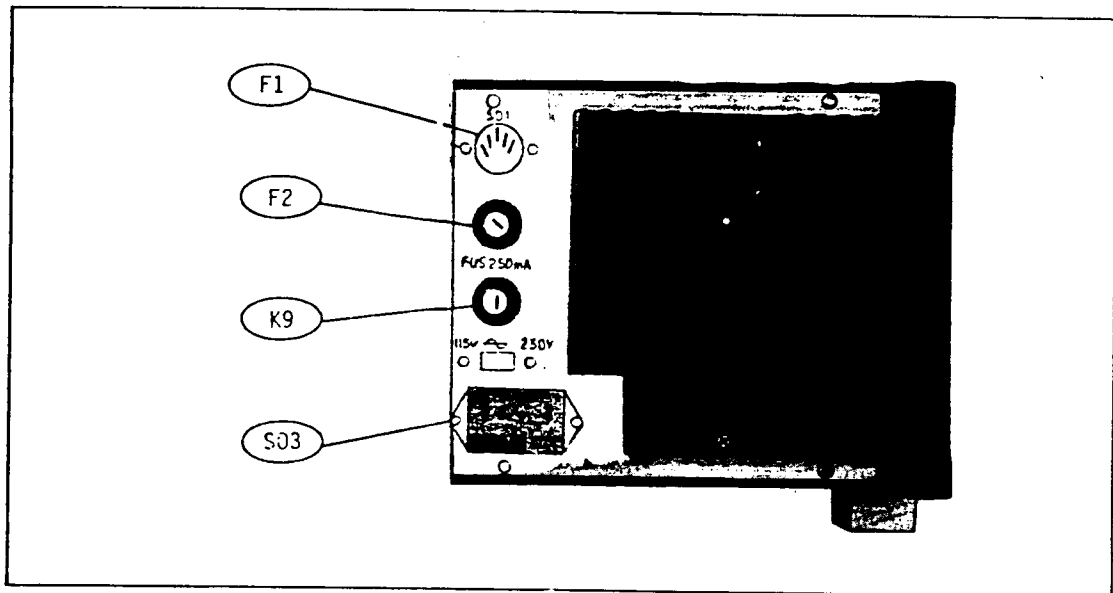
Figure IV-1 AC LINE CONNECTION

IV-2 MOUNTING IN 19" RACK

The instrument can be incorporated in a 19" rack thanks to two 3U adapters (reference 03 800064) delivered on request.
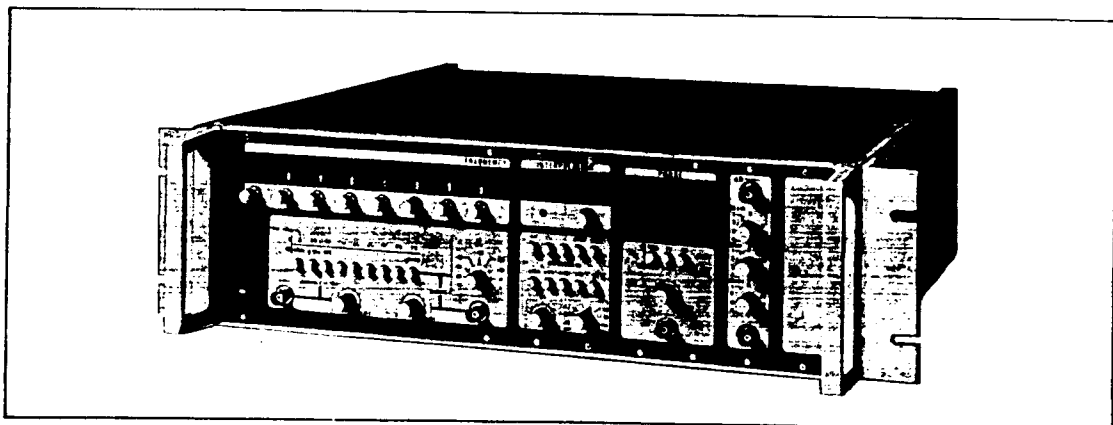
Figure IV-2 MOUNTING IN 19" RACK

V OPERATING INSTRUCTIONS

V-1 EXTERNAL DESCRIPTION

The different controls and connections on the front and rear panels of the 3100B synthesizer and its options are described on the following plates :

- Plate V-1 : front panel of the 3100B
- Plate V-2 : rear panel of the 3100B
- Plate V-3 : programmable attenuator option 3111B
- Plate V-4 : programmable phase-shifter option 3112B
- Plate V-5 : Search and Sweep option 3114B

V-2 3100B OPERATING INSTRUCTIONS

V-2-1 SWITCHING ON

The AC line voltage selector (K9) being in a position compatible with the mains voltage feeding the instrument, switching on is achieved by setting switch (K1) on position "1", which causes indicator (DS1) to light up.

V-2-2 LOCAL MODE

Selection of the Local mode is achieved by releasing "Local/Prog" key (K3) . The output frequency of the generator synthesizer is then controlled by the eight rotary switches (K2) .
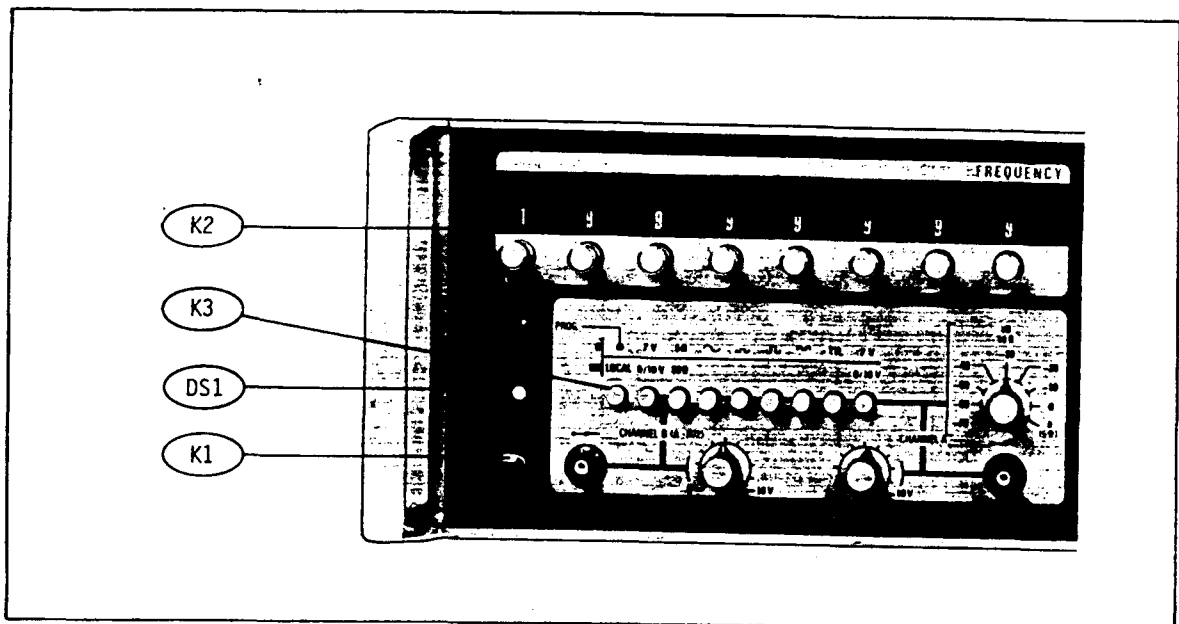
Figure V-1 LOCAL MODE

V-2-3 REMOTE MODE

Selection of the Remote mode is achieved either by pressing "Local/Prog" key (K3) or sending a "0" logic level to pin 17 of programming connector (S02) , the pin assignment of which is indicated in figure V-2.

Rotary switches (K2) are inhibited in Remote mode and the synthesized frequency programming is achieved in parallel BCD code through positive logic TTL signals sent to connector (S02).
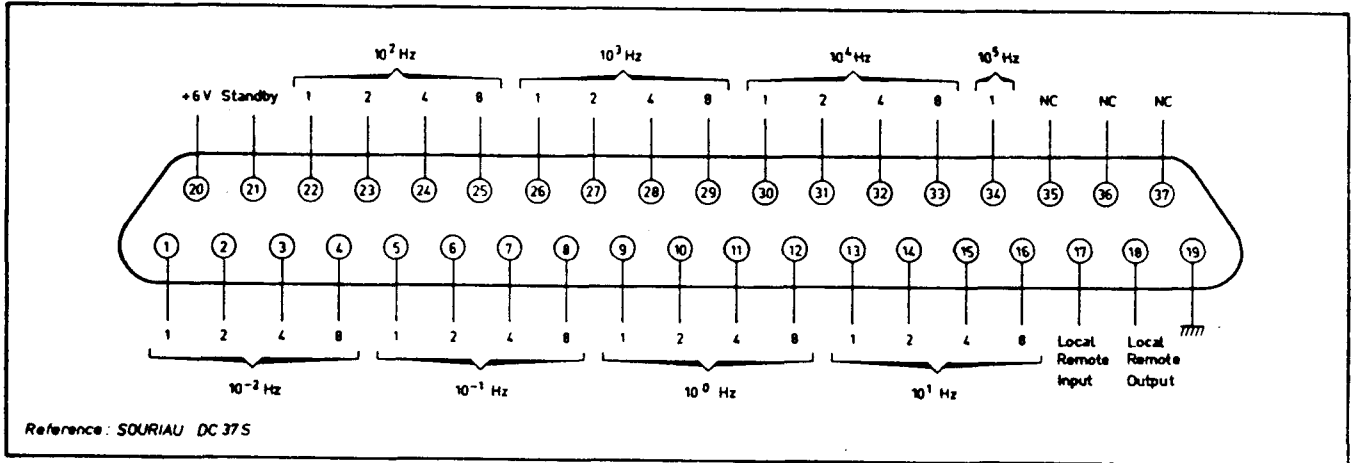
Figure V-2 PROGRAMMING CONNECTOR (S02)

Pin 18 of connector (S02) acts as a pilot of the Local/Remote mode of the 3100B synthesizer, as it delivers a + 6 V voltage in Remote mode and presents a high impedance in Local mode.

Pin 20 permanently supplies a + 6 V voltage which can facilitate programming and be used as a pilot of the instrument operation (maximum current : 50 mA).

Both in Local and Remote mode, grounding pin 21 inhibits the supply circuits, and the instrument ceases to function.

The input circuit of the programming signals consists of a low-power TTL gate preceded by an R-C filter, as shown in figure V-3.
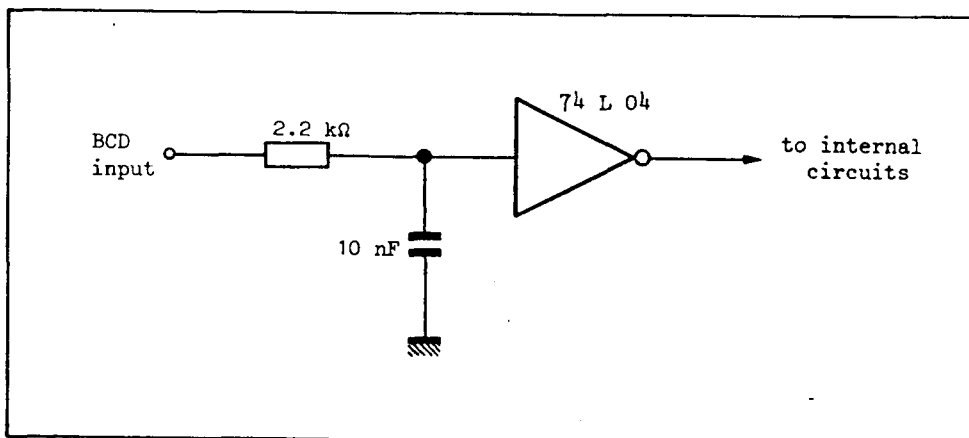
Figure V-3 PROGRAMMING SIGNAL INPUT CIRCUIT

V-2-4 OUTPUT SIGNALS

The 3100B generator synthesizer permanently delivers four synchronous signals on the following connectors :

<div style="margin-left: 2em">

Connector (J1) : main output A

Connector (J2) : main output B

Connector (J3) : auxiliary output A

Connector (J4) : auxiliary output B.

</div>

The output B signals present + 90° phase-shift with regard to the output A signals.
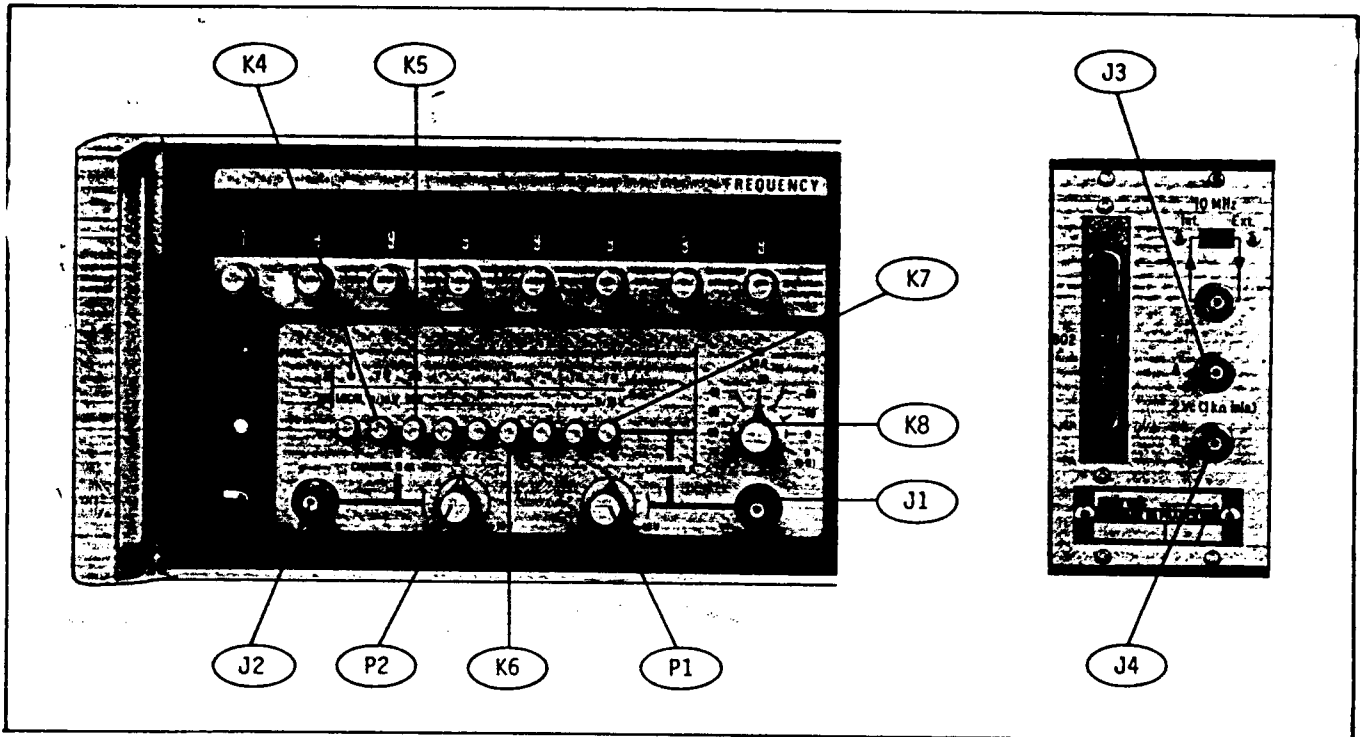
Figure V-4   OUTPUT SIGNALS


```
MAIN OUTPUT A
```
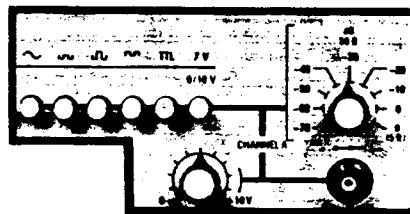
The main output A signal is available on connector (J1) in different shapes selected by keyboard (K6).

<div style="margin-left: 2em">

. Key ∿ : sine wave

. Key ⊔⊓⊔ : negative square wave

. Key ⊔⊓⊔ : symmetrical square wave (0 V mean value)

. Key ⊓⊔⊓ : positive square wave

. Key TTL : TTL square wave (0 V / 3.8 V).

</div>

Except for TTL level, the electromotive force of the signals delivered by connector (J1) depends on " 7V/10V " key (K7). This key allows to obtain either an e.m.f. calibrated at 7 Vpeak, or an e.m.f. variable from 0 V to 10 Vpeak depending on the setting of potentiometer (P1).

Switch (K8) provides selection of either a 5 Ω impedance without the possibility of attenuating the output level, or a 50 Ω impedance with an attenuation variable from 0 dB to 70 dB in 10 dB steps.

For example, a 700 mVp-p/50 Ω sine wave, which corresponds to 700 mVpeak e.m.f., is obtained by pressing " 7V/10V " key (K7) and key " ∿ " of keyboard (K6), and by setting switch (K8) on graduation "- 20".

TTL Level :

When a TTL square wave is selected on keyboard (K6), " 7V/10V " key (K7) and potentiometer (P1) are inhibited, but switch (K8) is still operating. To obtain a TTL level on connector (J1), it is then necessary to set switch (K8) on one of the two "0" graduations, so as to avoid an inopportune attenuation of the output signal.
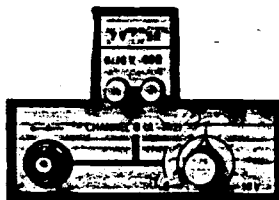
MAIN OUTPUT B

Main output B delivers on connector (J2) a sine wave phase-shifted from + 90° with regard to the main output A signal.

The (K4) " 7V/10V " key permits selection of either an e.m.f. calibrated at 7 Vpeak, or an e.m.f. adjustable from 0 V to 10 Vpeak through potentiometer (P2).

The output impedance is equal to 5 Ω or 50 Ω depending on whether "50 Ω/5 Ω" key (K5) is pressed or released.

AUXILIARY OUTPUT A

On connector (J3) at the rear of the instrument, auxiliary output A delivers a sine wave in phase with main output A.

The electromotive force of this output is about 2 Vpeak and its minimum load impedance is 1 kΩ .

AUXILIARY OUTPUT B

On connector (J4) at the rear of the instrument, auxiliary output B delivers a sine wave phase-shifted from + 90° with regard to main output A.

The electromotive force of this output is about 2 Vpeak and its minimum load impedance is 1 kΩ .

V-2-5 REFERENCE FREQUENCY

The synthesizer can be controlled either by the 10 MHz reference frequency delivered by the crystal oscillator of the Time Base, or by a 10 MHz external frequency.

When "Int./Ext." switch (K10) at the rear of the instrument is set on "Int.", the synthesizer is controlled by the 10 MHz reference frequency delivered by the Time Base. This frequency is then available on connector (J5) at a level of about 100 mVrms/50 Ω.

Control by external reference is achieved by setting switch (K10) on "Ext." and by sending on connector (J5) a 10 MHz frequency at 50 mV rms/50 Ω to 1 V rms/50 Ω input level. In this case, the frequency delivered by the different outputs of the synthesizer has the same stability as the frequency applied to connector (J5).
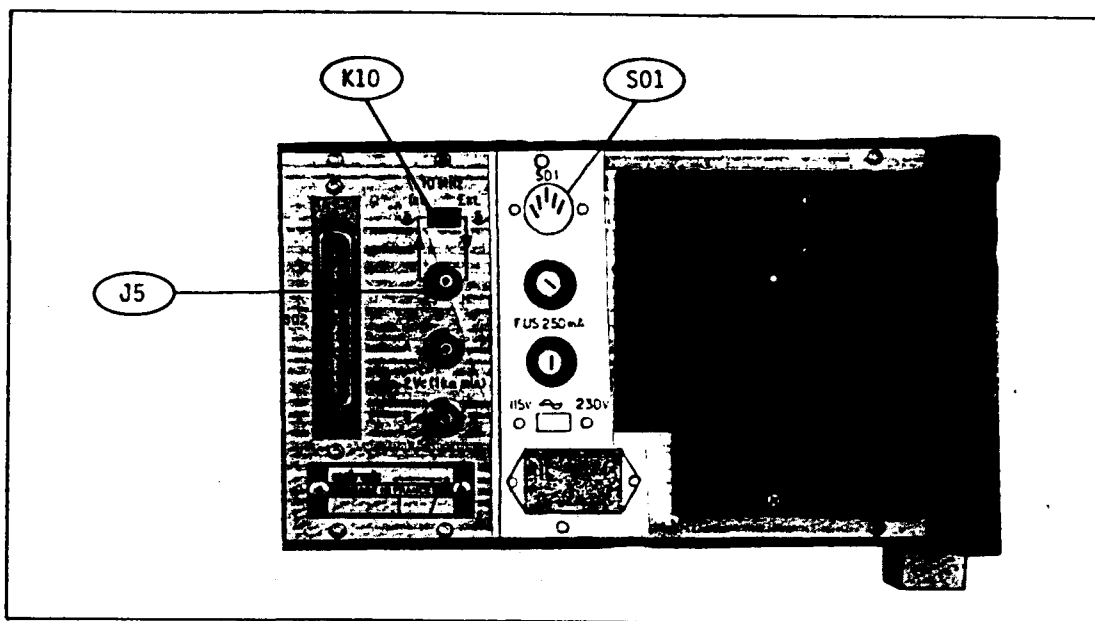
Figure V-5 REFERENCE FREQUENCY

V-2-6 SUPPLY VOLTAGES OUTPUT

Socket (S01), whose pin assignment is indicated in figure V-6, provides + 12 V, + 6 V and - 12 V regulated voltages aimed at feeding external circuits.

Maximum current for each voltage : 20 mA.
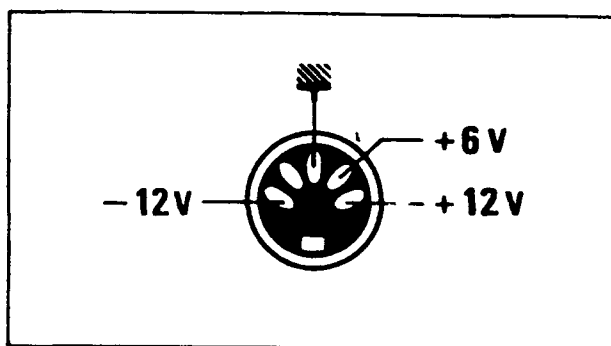
Figure V-6 SOCKET (S01)

The 3111B option is a programmable attenuator which provides an attenuation variable from 0 to 79.9 dB in 0.1 dB steps.

Connector (J11) constitutes the attenuator input and connector (J12) constitutes its outputs.
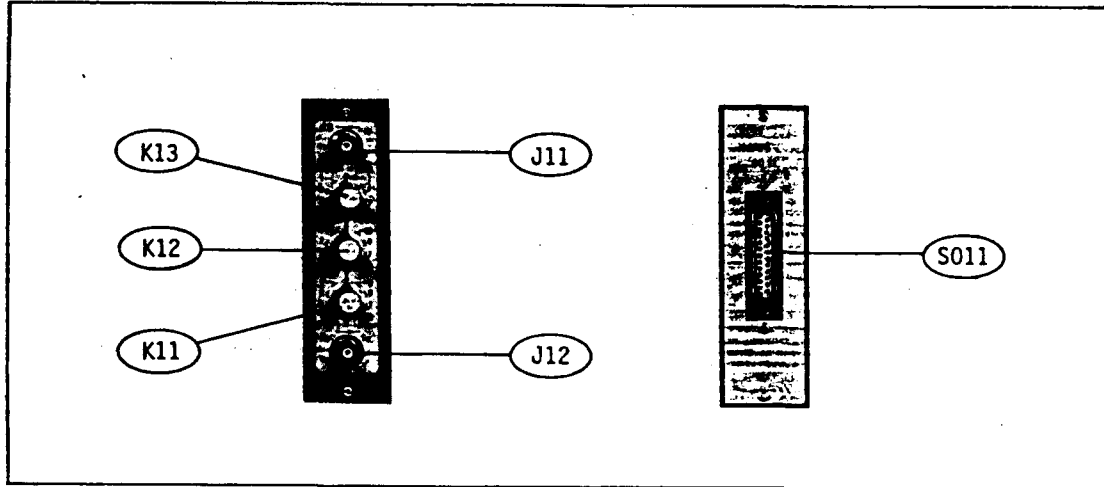
Figure V-7   PROGRAMMABLE ATTENUATOR 3111B

V-3-1   LOCAL MODE

The Local mode is automatically selected by setting 10 dB steps switch (K13) on one of graduations "0" to "7". The 0.1 dB and 1 dB steps of the attenuation are then controlled by switches (K11) and (K12) respectively.

V-3-2   REMOTE MODE

The selection of the Remote mode is achieved either by setting switch (K13) on the red dot, or by sending a "0" logic level on pin 16 of programming connector (S011) , the pin assignment of which is indicated in figure V-8.
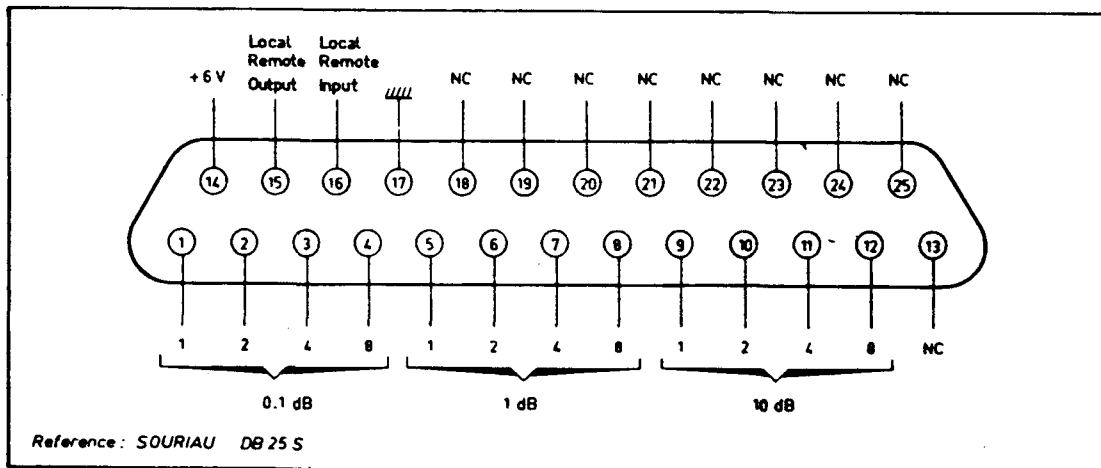
Figure V-8   PROGRAMMING CONNECTOR (S011)

The attenuation programming is achieved in parallel BCD code through positive logic TTL signals sent on connector (S011) . As for the programming of the synthesized frequency, the input circuit of the programming signals consists of a low-power TTL gate preceded by an R-C filter (see figure V-3 in section V-2-3).

Pin 15 of connector (S011) acts as a pilot for the Local/Remote mode of the 3111B programmable attenuator, as it delivers a + 6 V voltage in Remote mode and presents a high impedance in local mode.

Pin 14 permanently supplies a + 6 V voltage which can facilitate the attenuation programming (maximum current : 50 mA).

V-4   3112B OPERATING INSTRUCTIONS

The 3112B plug-in is a programmable phase-shifter which delivers a sine wave phase-shifted from 0° to 359.9° with regard to the signal delivered by main output A of the 3100B synthesizer.
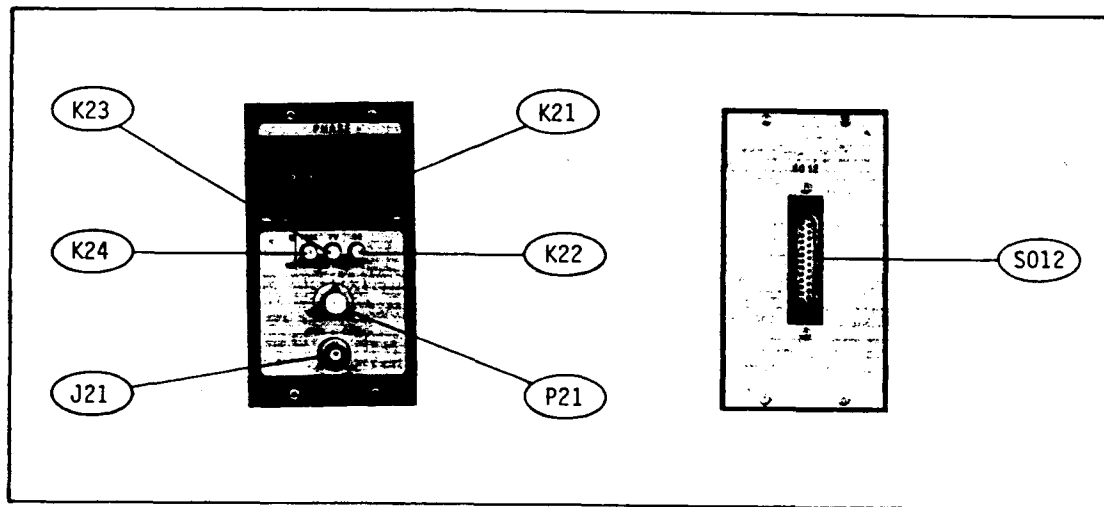
Figure V-9   PROGRAMMABLE PHASE-SHIFTER 3112B

V-4-1   LOCAL MODE

The selection of the Local mode is achieved by releasing "Local/Prog" key (K24). The phase-shift of the signal delivered by connector (J21) is then controlled by four thumbwheel switches (K21) .

V-4-2 REMOTE MODE

The selection of the Remote mode is achieved either by pressing "Local/Prog" key (K24), or by sending a "0" logic level on pin 16 of programming connector (S012) , the pin assignment of which is indicated in figure V-10.
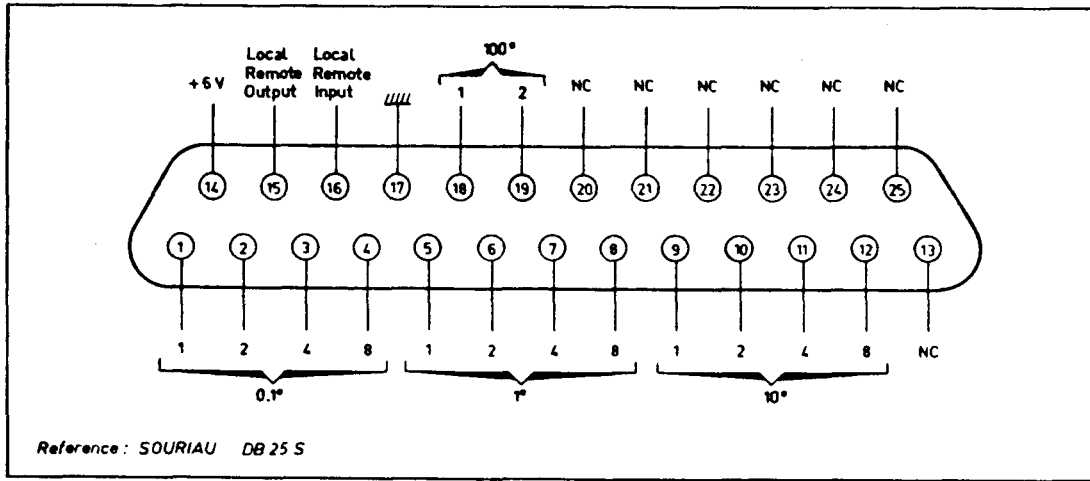
Figure V-10 PROGRAMMING CONNECTOR (S012)

Thumbwheel switches (K21) are inhibited in Remote mode and the phase-shift programming is achieved in parallel BCD code through positive logic TTL signals sent on connector (S012) . As for the synthesized frequency programming, the input circuit of the programming signals consists of a low-power TTL gate preceded by a R-C filter (see figure V-3 in section V-2-3).

Pin 15 of connector (S012) acts as a pilot for the Local/Remote mode of the 3112B programmable phase-shifter, as it delivers a + 6 V voltage in Remote mode and presents a high impedance in Local Mode.

Pin 14 permanently supplies a + 6 V voltage which can facilitate the phase-shift programming (maximum current : 50 mA).

V-4-3 OUTPUT SIGNAL

The phase-shifted signal is available on connector (J21) at 5 Ω or 50 Ω output impedance, depending whether "50 Ω/5 Ω" key (K22) is pressed or released.

The (K23) " 7V/10V " key permits selection of either an e.m.f. calibrated at 7 Vpeak, or an e.m.f. adjustable from 0 V to 10 Vpeak through potentiometer (P21).

The 3114B Search and Sweep option provides continuous variation of the frequency delivered by the 3100B generator synthesizer and the 3112B programmable phase-shifter. This variation can be achieved according to four distinct modes : Search function, Free-run Sweep, Triggered Sweep, External mode.

V-5-1   SEARCH FUNCTION

This operating mode is obtained by leaving the three keys of keyboard (K41) in released position and permits a continuous variation of the synthesizer output frequency within a preselected interpolation range ($\pm$ 1 Hz, $\pm$ 10 Hz, $\pm$ 100 Hz, $\pm$ 1 kHz or $\pm$ 10 kHz).
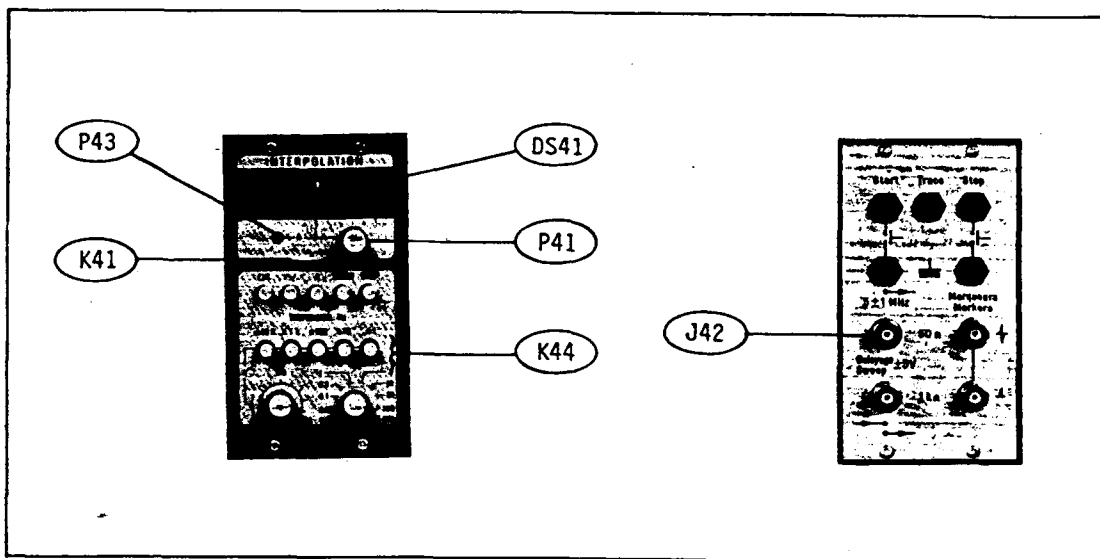
Figure V-11   SEARCH FUNCTION

The interpolation range is selected by "Dispersion" keyboard (K44) and is displayed on the front panel of the 3100B synthesizer through indicators (DS2) showing the inhibition of the digits of a weight inferior to this range. For example, the $\pm$ 10 Hz range selection inhibits the 1 Hz, 0.1 Hz and 0.01 Hz digits and lights up indicator (DS2) between the switches of the 1 Hz and 10 Hz digits.

An interpolation range being selected, potentiometer (P41) provides continuous variation of the synthesizer output frequency. The value of this variation is displayed on linear scale (DS41), whose "-1" and "+1" extreme graduations correspond to the entire interpolation range selected.

5 MHz $\pm$ 1 MHz OUTPUT

The output frequency interpolation is represented by the 5 MHz $\pm$ 1 MHz frequency available on connector (J42) at a level of about 200 mVrms/50 Ω. This frequency varies by $\pm$ 1 MHz for the entire interpolation range selected, which allows very accurate measurement of the synthesizer output frequency with a low-resolution frequencymeter.

For example, measuring the 5 MHz $\pm$ 1 MHz frequency with a four-digit frequencymeter provides 10^{-4} Hz resolution when the interpolation range is fixed at $\pm$ 1 Hz. If the synthesizer output frequency is 100 kHz, the relative resolution thus reaches 10^{-9}.

As the 5 MHz $\pm$ 1 MHz frequency is generated through arithmetical operations between the frequency delivered by the interpolation oscillator and the 10 MHz reference issued from the Time Base, the deviation of this 5 MHz $\pm$ 1 MHz frequency is always exactly proportional to the interpolation of the synthesizer output frequency. The proportionality factor varies from 10^2 for the $\pm$ 10 kHz range to 10^6 for the + 1 Hz range.

INTERPOLATION OSCILLATOR CENTERING

Adjustment potentiometer (P43) allows the "0" graduation of linear scale (DS41) to coincide with the 5 MHz frequency delivered by connector (J42) when the output interpolation is nil, as shown in fig. V-12.
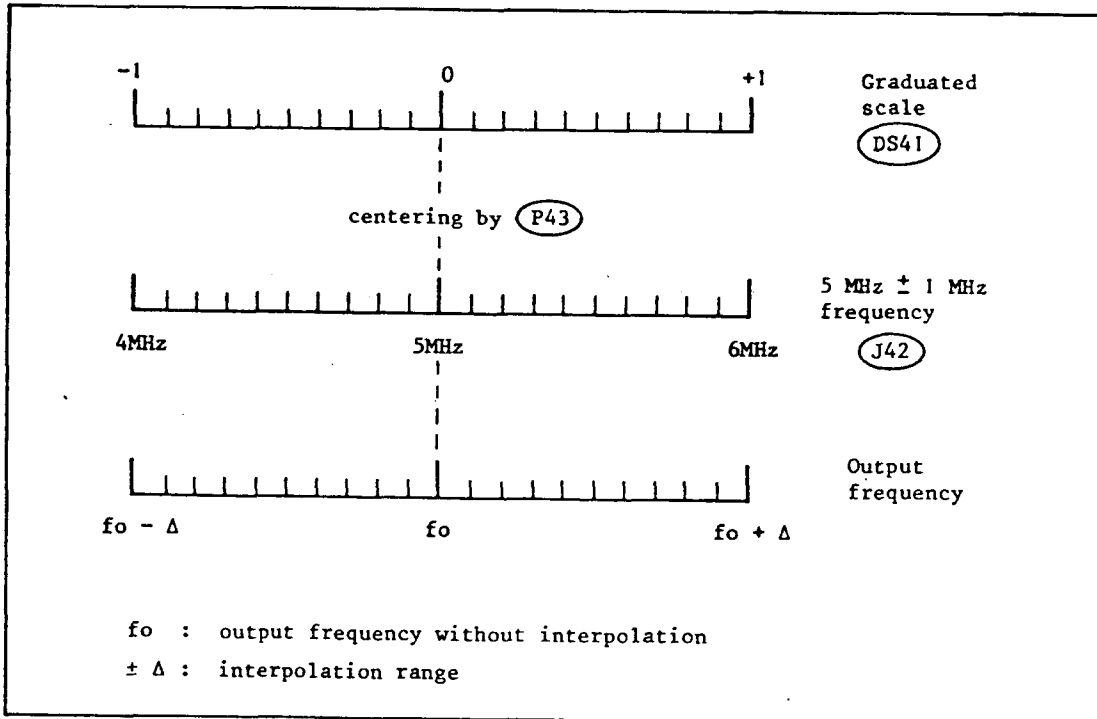
Figure V-12 INTERPOLATION OSCILLATOR

V-5-2 FREE-RUN MODE

This operating mode, controlled by the "/\/" key of keyboard (K41), provides an output frequency sweep to the generator synthesizer through symmetrical triangular signals.
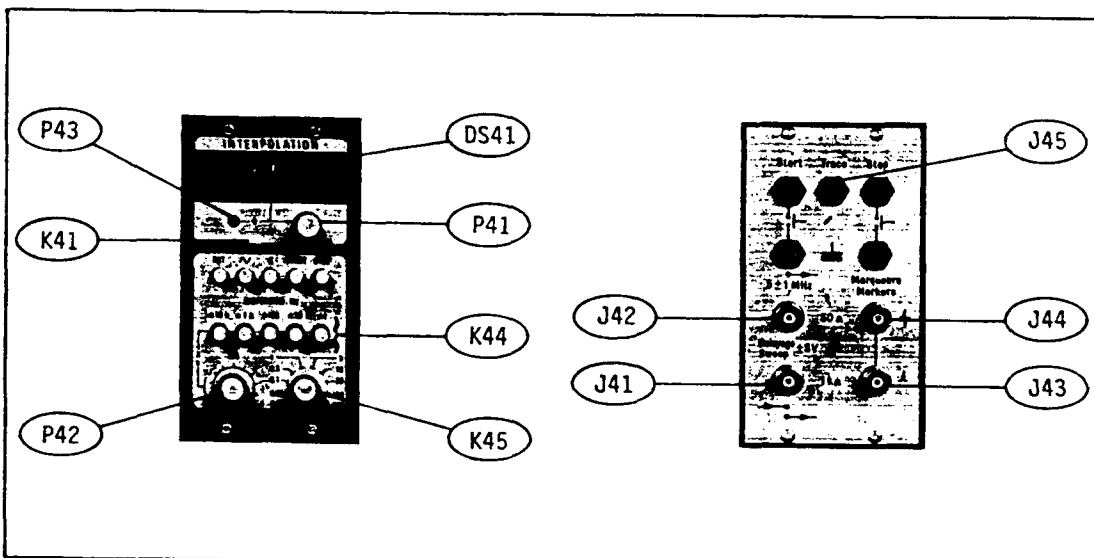
Figure V-13 FREE-RUN MODE

SWEEP

Sweep duration, equal to the half period of the symmetrical sweep signals, is adjustable from 10 ms to 300 s through switch (K45) .

The symmetrical triangular sweep signals are available on connector (J41) with ± 5 V amplitude, the minimal load impedance being 1 kΩ.

During the rise of triangular sweep signals, socket (J45) presents a low impedance, which can sink a 50 mA current. When the triangular sweep signals fall from + 5 V to - 5 V, this socket delivers a + 12 V voltage with high impedance.

DISPERSION

The dispersion range is selected on keyboard (K44) and displayed on the 3100B front panel through indicators (DS2) showing the inhibition of the digits of a weight inferior to this range.

Potentiometer (P42) permits adjustment of the frequency deviation within the dispersion range. For example, the adjustment of this potentiometer at half-way provides ± 5 Hz sweep around the center frequency when the dispersion range selected by keyboard (K44) is ± 10 Hz.

The center frequency around which the sweep is achieved is determined by potentiometer (P41) and its value is displayed on linear scale (DS41), whose "+1" and "-1" extreme graduations correspond to the entire dispersion range.

It should be noted that the total variation introduced by the center frequency offset and by the sweep width must never exceed the dispersion range value. For example, when the dispersion range is fixed at ± 10 Hz, if potentiometer (P41) provides + 8 Hz offset, the sweep width determined by potentiometer (P42) must not exceed ± 2 Hz.

5 MHz ± 1 MHz OUTPUT

Connector (J42) delivers at an approximate level of 200 mVrms/50 Ω a 5 MHz ± 1 MHz frequency which represents the variation of the synthesizer output frequency with ± 1 MHz deviation for the whole dispersion range selected. For example, when the dispersion range is ± 10 Hz, if potentiometer (P41) provides + 2 Hz center frequency offset and if the sweep width is fixed at ± 5 Hz by potentiometer (P42) , the frequency delivered by connector (J42) varies from 4.7 MHz to 5.7 MHz at the sweep rate.

The 5 MHz ± 1 MHz frequency is generated through arithmetical operations between the frequency delivered by the interpolation oscillator and the 10 MHz reference issued from the synthesizer Time Base. The deviation of this frequency with respect to 5 MHz is thus exactly proportional to the total variation of the synthesizer output frequency.

INTERPOLATION OSCILLATOR CENTERING

Adjustment potentiometer (P43) allows the "0" graduation of linear scale (DS41) to coincide with the 5 MHz frequency delivered by connector (J42) when the variation of the synthesizer output frequency is nil (see figure V-12, section V-5-1).

```
   BIRDY MARKERS                          RECTIFIED MARKERS




fo - Δ          fo         fo + Δ      fo - Δ          fo         fo + Δ

fo  : center frequency
± Δ : dispersion range
```

Figure V-14   MARKER SPACING

Connector (J44) delivers 21 "birdy" markers spaced every 10 % of the dispersion range. The center and the ends of the dispersion range are marked with three markers of about 500 mVp-p/50 Ω amplitude, whilst the other eighteen markers have an amplitude of approximately 100 mVp-p/50 Ω.

Connector (J43) delivers 21 rectified markers more particularly suited to X-Y recorders. As for the "birdy" markers, the space between two markers is equal to 10 % of the dispersion range. The center and the ends of the dispersion range are marked with three markers of about 500 mVpeak e.m.f., whilst the other eighteen markers have approximately 100 mVpeak e.m.f., the minimal load impedance being 1 kΩ.

V-5-3 TRIGGERED MODE

This operating mode, controlled by the "⟋⎳" key of keyboard (K41), provides a sawtooth sweep of the generator synthesizer output frequency.
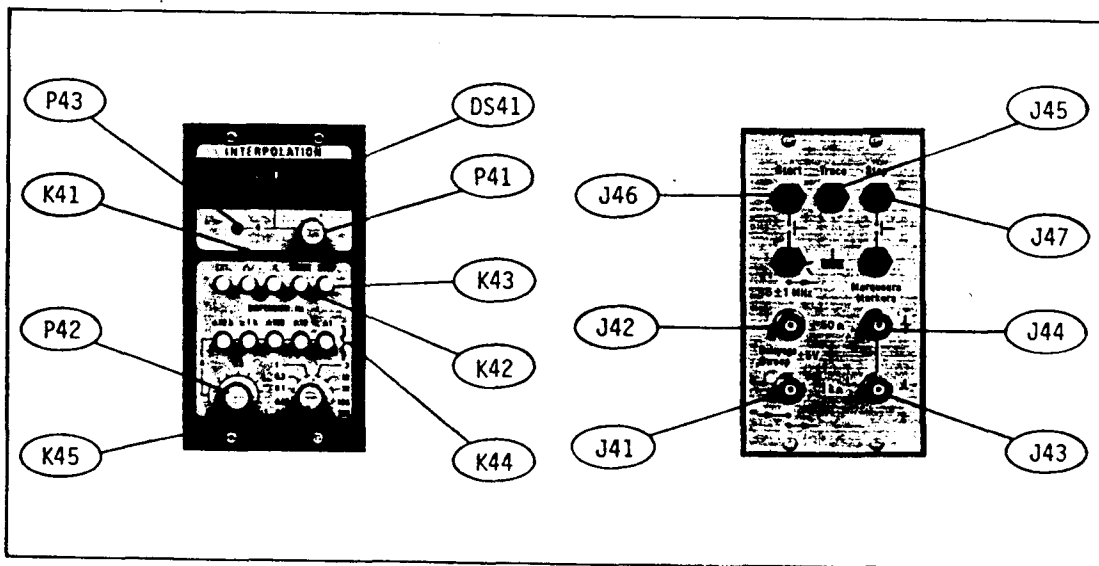
Figure V-15   TRIGGERED MODE

SWEEP

The start of the sawtooth effecting the sweep can be controlled either by pressing key (K42) or by grounding socket (J46) on the rear panel of the instrument.

The duration of this sawtooth is adjustable from 10 ms to 300 s through switch (K45). However, pressing key (K43) or grounding socket (J47) will get the sawtooth back to its starting point before the duration fixed by switch (K45).

This sawtooth is available on connector (J41) with ± 5 V amplitude, in so far as it is not brought back to its - 5 V starting point before the duration fixed by (K45). The minimal load impedance that connector (J41) can receive is 1 kΩ.

When the sawtooth rises, socket (J45) exhibits a low impedance which can sink a 50 mA current. When the sawtooth gets back to its starting point, this socket delivers a + 12 V voltage with high impedance.

DISPERSION

The dispersion range is selected on keyboard (K44) and is displayed on the front panel of the 3100B through indicators (DS2) showing the inhibition of the digits having a weight inferior to this range.

Potentiometer (P42) allows continuous adjustment of the sweep width within the dispersion range. For example, the adjustment at half-way of this potentiometer provides a ± 5 Hz sweep around the center frequency when the dispersion range selected by keyboard (K44) is ± 10 Hz.

The center frequency around which the sweep is achieved is determined by potentiometer (P41) and its value is displayed on linear scale (DS41) whose "+1" and "-1" extreme graduations correspond to the whole dispersion range.

It should be noted that the total variation brought by the center frequency offset and by the sweep width must never exceed the dispersion range value. For example, when the dispersion range is fixed at ± 10 Hz, if potentiometer (P41) brings + 8 Hz offset, the sweep width determined by potentiometer (P42) must not exceed ± 2 Hz.

5 MHz ± 1 MHz OUTPUT

Connector (J42) delivers at an approximate level of 200 mVrms/50 Ω a 5 MHz ± 1 MHz frequency representing the variation of the synthesizer output frequency with ± 1 MHz deviation for the whole dispersion range selected. For example, when the dispersion range is ± 10 Hz, if potentiometer (P41) provides + 2 Hz center frequency offset and if the sweep is fixed at ± 5 Hz by potentiometer (P42), the frequency delivered by connector (J42) varies from 4.7 MHz to 5.7 MHz at the sweep rate.

The 5 MHz ± 1 MHz frequency is generated through arithmetical operations between the frequency delivered by the interpolation oscillator and the 10 MHz reference issued from the synthesizer Time Base. The deviation of this frequency with respect to 5 MHz is thus exactly proportional to the total variation of the synthesizer output frequency.

INTERPOLATION OSCILLATOR CENTERING

Adjustment potentiometer (P43) allows the "0" graduation of linear scale (DS41) to coincide with the 5 MHz frequency delivered by connector (J42) when the variation of the synthesizer output frequency is nil (see figure V-12, section V-5-1).
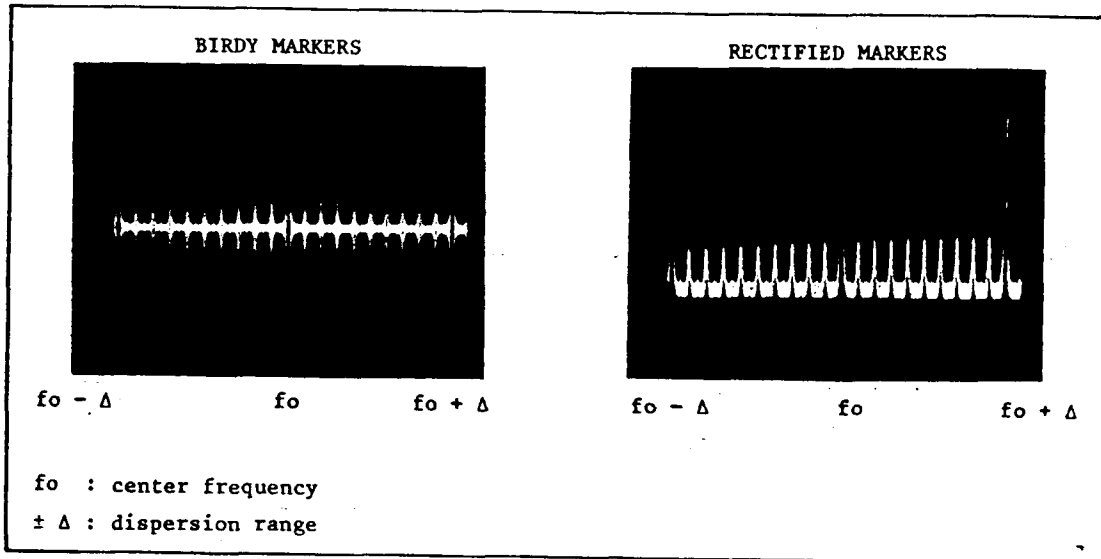
MARKERS

As in free-run mode, connectors (J43) and (J44) respectively deliver rectified markers and "birdy" markers spaced every 10 % of the dispersion range (see section V-5-2).

V-5-4 EXTERNAL MODE

This operating mode controlled by the "Ext." key of keyboard (K41) makes possible the Search or Sweep of the synthesizer output frequency by means of an external signal.
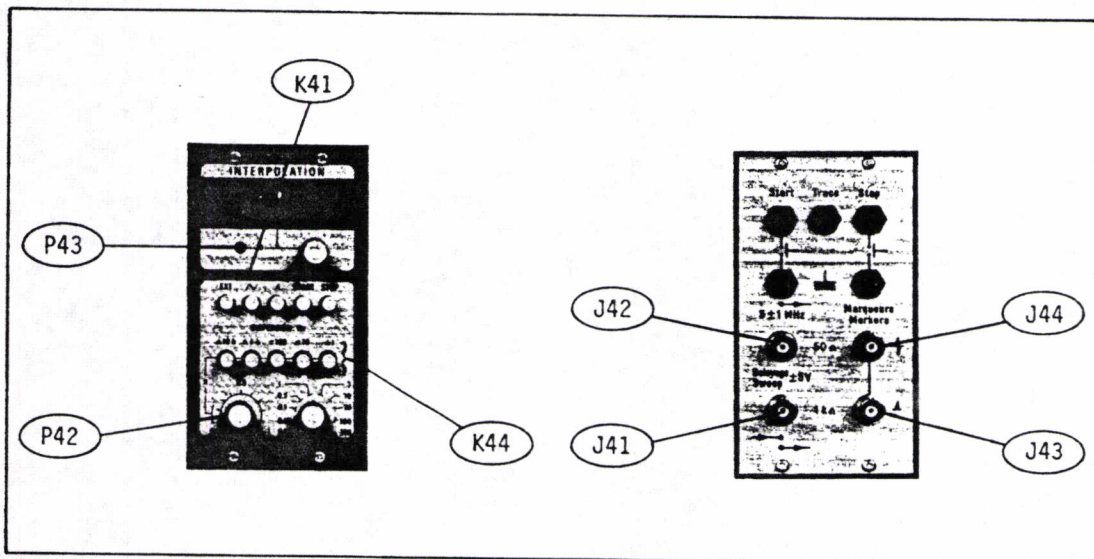
Figure V-16 EXTERNAL MODE

SWEEP INPUT

The search or sweep of the synthesizer output frequency is achieved by sending a - 5 V to + 5 V external voltage on connector (J41) which, in this case, presents 10 kΩ input impedance.

DISPERSION

The dispersion range is selected on keyboard (K44) and is displayed on the front panel of the 3100B through indicators (DS2), showing the inhibition of the digits having a weight inferior to this range.

A dispersion range being selected, the frequency variation depends both on the amplitude of the signal applied to connector (J41) and on the position on which potentiometer (P42) is set. To obtain a frequency variation equal to the whole dispersion range, the amplitude of the signal applied to connector (J41) must be ± 5 V and potentiometer (P42) must be set on the extreme right position.

5 MHz ± 1 MHz OUTPUT

Connector (J42) delivers at an approximate level of 200 mVrms/50 Ω a 5 MHz ± 1 MHz frequency which represents the variation of the synthesizer output frequency with ± 1 MHz deviation for the whole dispersion range selected.

As the 5 MHz ± 1 MHz frequency is generated through arithmetical operations between the frequency delivered by the interpolation oscillator and the 10 MHz reference issued from the synthesizer Time Base, the deviation of this frequency with respect to 5 MHz is exactly proportional to the variation of the synthesizer output frequency.

INTERPOLATION OSCILLATOR CENTERING .

Split-shaft potentiometer (P43) permits centering of the interpolation oscillator, so that the "5 MHz ± 1 MHz" output (J42) delivers a 5 MHz frequency when no signal is applied to connector (J41).

MARKERS

As in free-run mode, connectors (J43) and (J44) respectively deliver rectified markers and "birdy" markers spaced every 10 % of the dispersion range (see section V-5-2).

VI CIRCUIT DESCRIPTION

VI-1 INTRODUCTION

The operation of the 3100B ADRET generator synthesizer is based on the indirect frequency synthesis, making use of phase-locked loops composed of a voltage-controlled oscillator, a programmable counter and a phase comparator, as shown in figure VI-1.
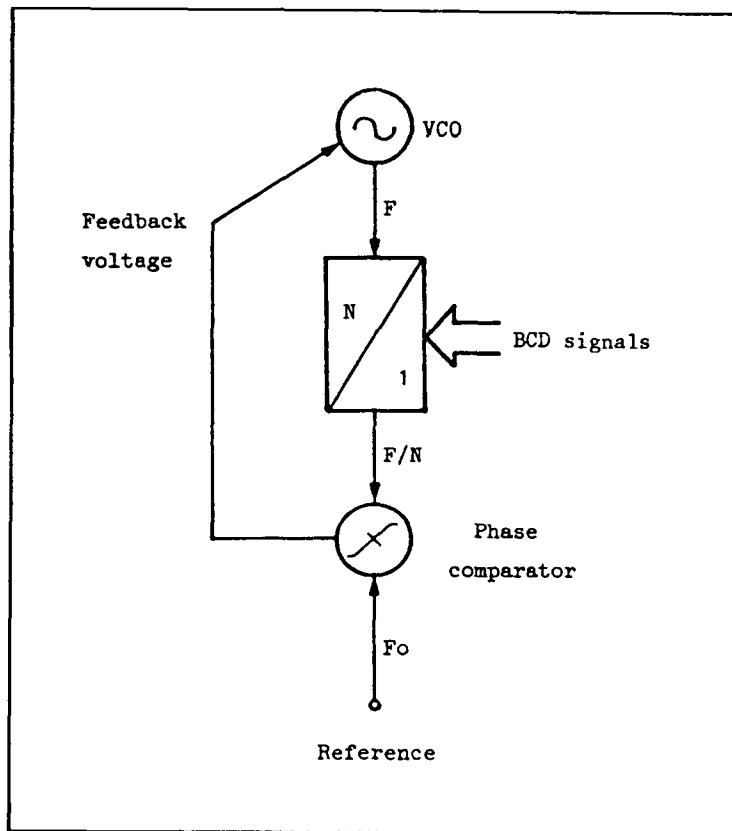
Figure VI-1 PHASE-LOCKED LOOP PRINCIPLE

The F frequency delivered by the oscillator is applied to the programmable counter, the N division rate of which is controlled by BCD programming signals. The F/N frequency provided by the programmable counter is then compared to an F_0 reference frequency in the phase comparator, which gives a phase-locking voltage allowing to maintain the F frequency of the oscillator equal to N times the F_0 reference.

Such a phase-locked loop can thus generate ten different frequencies multiple of F_0 when the N division rate of the programmable counter has ten different values.

See block diagram on plate VI-1 and figure VI-2, as well as schematic on plate VI-3.
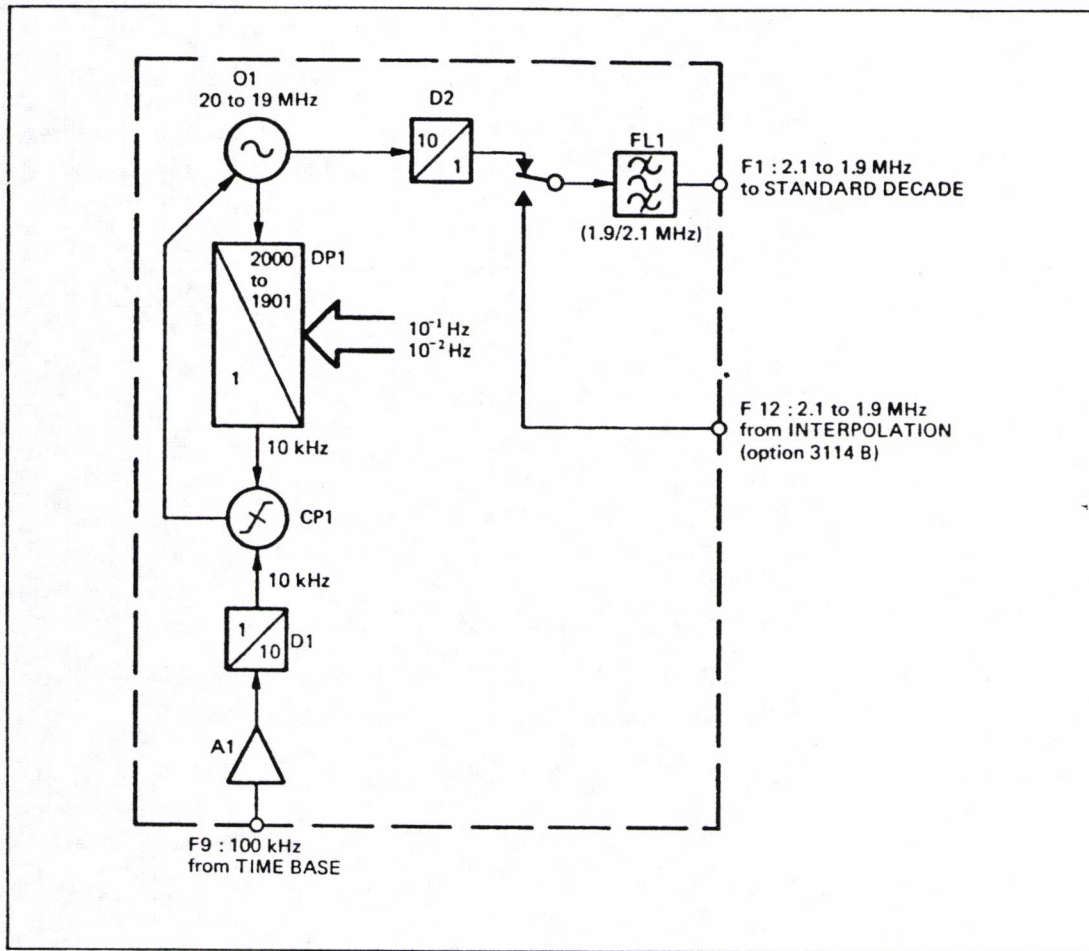
Figure VI-2   CENTADE

This subassembly elaborates the 10^{-2} Hz and 10^{-1} Hz increments of the output frequency, by means of a phase-locked loop consisting of oscillator O1, programmable counter DP1 and phase-frequency comparator CP1.

Oscillator O1 generates a 19.01 MHz to 20 MHz frequency divided by the N division rate of programmable counter DP1. The frequency delivered by this counter DP1 is then compared in phase/frequency comparator CP1 with a 10 kHz reference, obtained by dividing by 10 frequency F9 : 100 kHz issued from the Time Base. Comparator CP1 thus provides a DC voltage phase-locking oscillator O1 to a frequency equal to N times the 10 kHz reference frequency.

The frequency generated by oscillator O1 is divided by 10 in divider D2, then filtered in band-pass filter FL1 before being sent to the first Standard Decade.

When an interpolation range is selected on option 3114B, the + 6 V supply voltage of the Centade is cut off. Besides, if the interpolation range is ± 1 Hz, frequency F12 : 2.1 MHz/1.9 MHz is substituted at filter FL1 for the synthesized frequency (see section VI-11).

PRINCIPLE OF PROGRAMMABLE COUNTER DP1
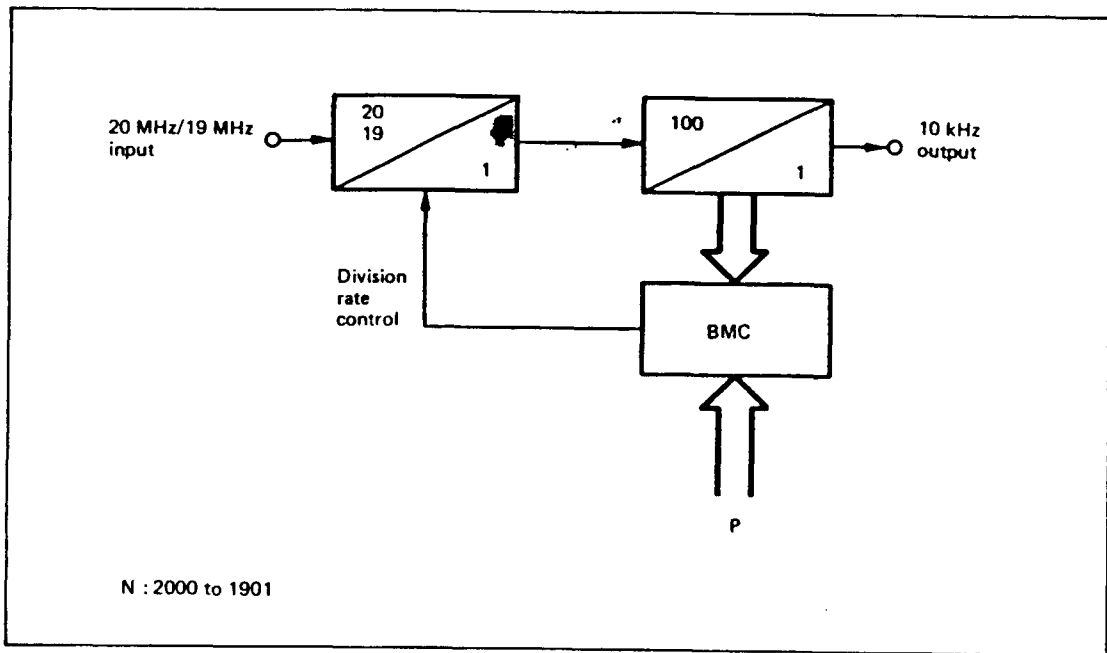
Figure VI-3   PRINCIPLE OF COUNTER DP1

Programmable counter DP1 mainly comprises a divider by 19 or 20, a fixed divider by 100 and a Binary Module Comparator. This latter compares the state of the fixed divider with the value P : 0 to 99 of the programming signals and determines the division rate of the front divider, equal to 19 as long as the state of the fixed divider is inferior to P, and equal to 20 during the remaining of the counting cycle.

The overall division rate N : 2000 to 1901 of counter DP1 is thus expressed as follows :

$$N = 19 \, P + 20 \, (100 - P)$$

The divider by 100 consists of two 74 LS 90 decades (integrated circuits SN5 and SN6, plate VI-3). The divider by 19 or 20 consists of a 7495 shift-register mounted as a divider by 4 or 5 (integrated circuit SN2), two J-K flip-flops mounted as a divider by 4 (integrated circuit SN4) and NAND gates (integrated circuit SN3) allowing the division rate of the whole unit to be fixed at 19 or 20.

The Binary Module Comparator consists of a coincidence circuit (integrated circuits SN7, SN8 and SN9) followed by a J-K flip-flop (integrated circuit SN10) delivering the control information to the front divider.

PRINCIPLE OF THE PHASE/FREQUENCY COMPARATOR

The principle of the phase/frequency comparator consists in generating pulses with a width proportional to the phase-shift of the two signals compared, then in integrating these pulses so as to obtain a DC voltage permitting the phase-locking of an oscillator.

When the F_0 and F_x compared frequencies are identical, the phase/frequency comparator operates like a phase comparator. When these two frequencies are unequal, the phase/frequency comparator indicates which one is larger, whence its appellation "phase/frequency comparator".

As shown in figure VI-4, the digital part of the phase/frequency comparator consists of two J-K flip-flops, the Q1 and Q2 outputs of which are applied to a NAND gate reacting on the Clear input of each flip-flop.
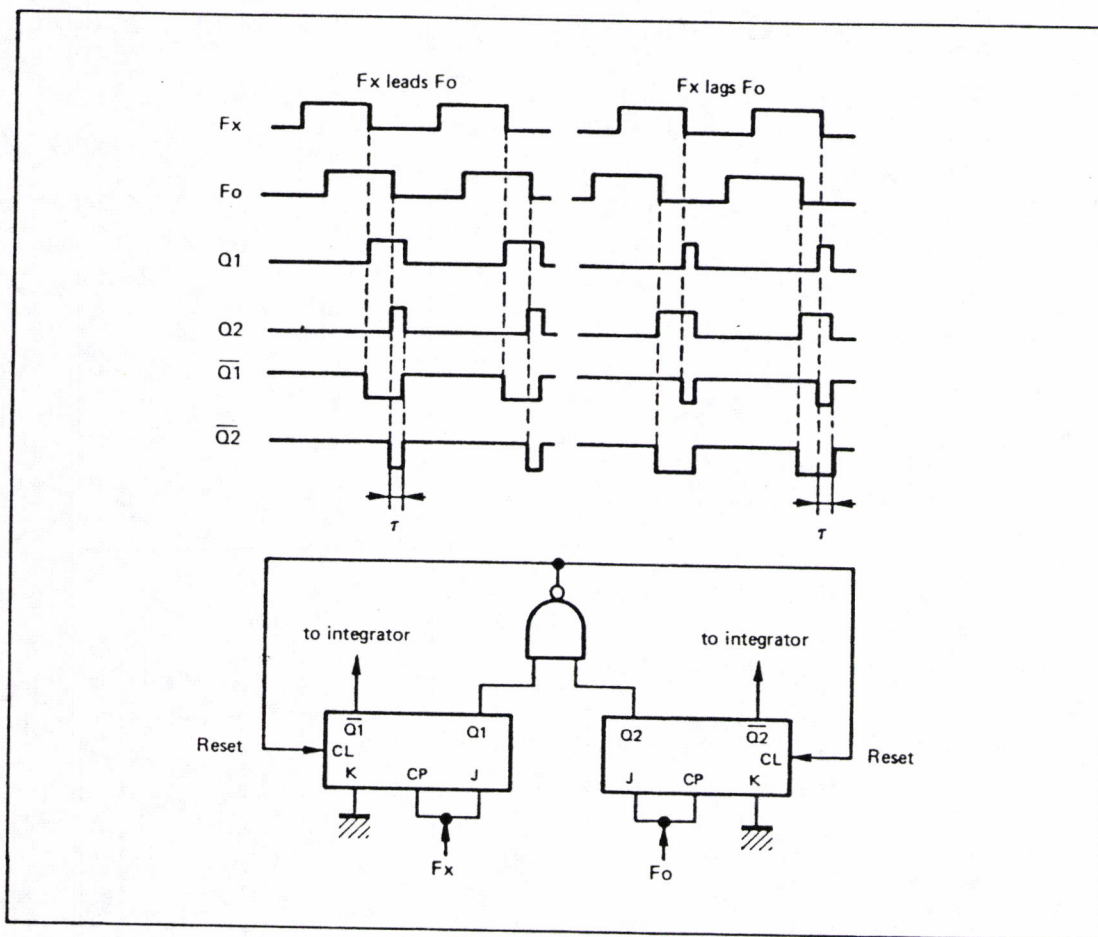
Figure VI-4 PHASE/FREQUENCY COMPARATOR

The F_0 and F_x signals to be compared are applied to the CP and J inputs of each flip-flop. Since the K inputs are grounded, the negative-going edges of each of the F_0 and F_x signals bring about a "1" logic level on the Q output of the corresponding flip-flop. On account of the reaction of the NAND gate on the Clear inputs, the Q1 and Q2 outputs return to the "0" state once they have both reached the "1" state, after a short time equal to the propagation time of the NAND gate. In practice, two interters are cascaded with the NAND gate, in order to provide a longer propagation time and thereby a larger output pulse width.

The width difference between the pulses delivered by the Q1 and Q2 outputs is thus proportional to the phase-shift between the F_0 and F_x signals. A DC voltage proportional to this phase-shift is then obtained by integrating the output pulses through the differential integrator composed of transistors Q4, Q5 and Q6.

See block diagram on plate VI-1 and figure VI-5, as well as schematic on plate VI-4.
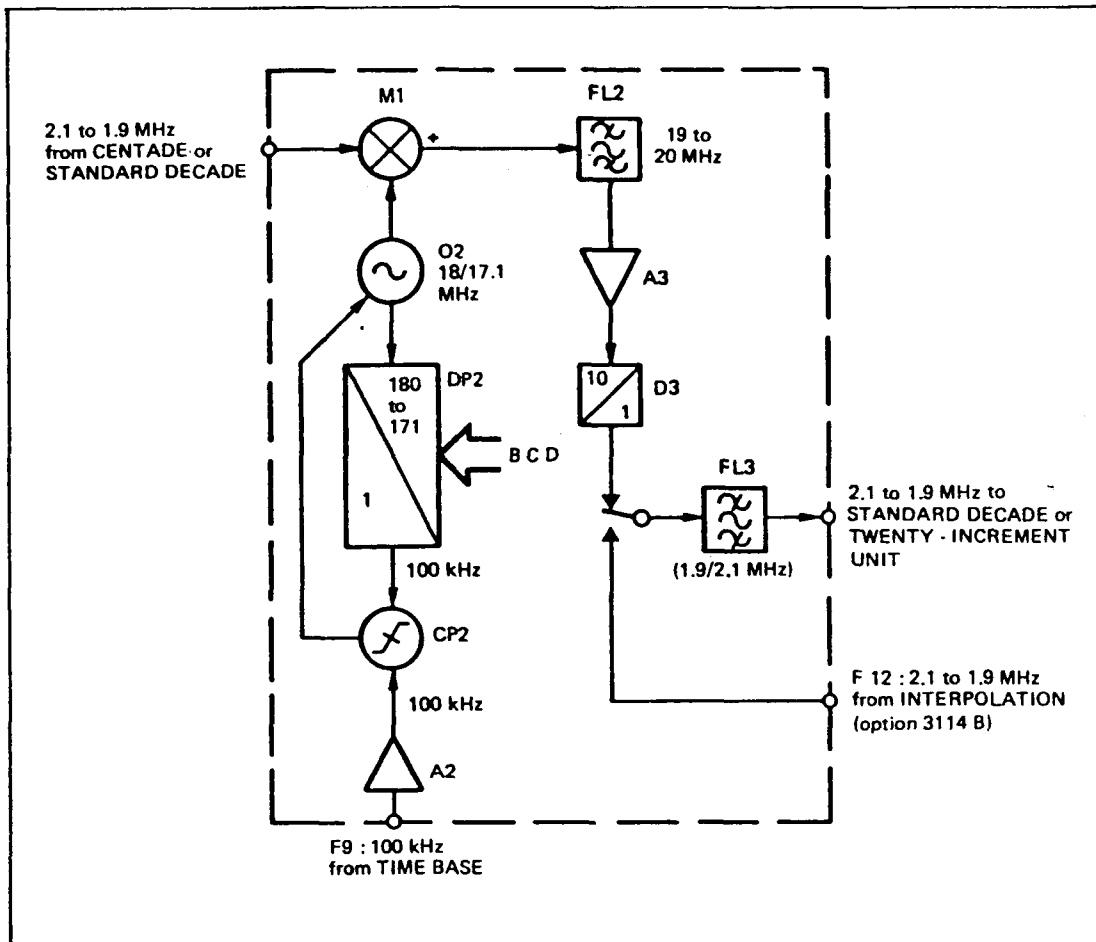
Figure VI-5 STANDARD DECADE

Each Standard Decade comprises a phase-locked loop elaborating ten frequency steps, together with mixing circuits allowing the incorporation of frequency steps elaborated in the preceding Decades.

Oscillator O2 delivers an 18 MHz to 17.1 MHz frequency, divided by N : 180 to 171 in programmable divider DP2. The output frequency of DP2 is then compared to reference frequency F9 : 100 kHz coming from Time Base in phase/frequency comparator CP2, which provides a feedback voltage keeping the frequency of oscillator O2 equal to N times 100 kHz. Since N varies from 180 to 171 according to the BCD programming signals applied to DP2, this phase-locked loop elaborates ten 100-kHz frequency steps.

The 18 MHz to 17.1 MHz frequency generated by oscillator O2 is fed to mixer M1, receiving on the other hand frequency F1, F2, F3 or F4 from the Centade or from the preceding Standard Decade. Filter FL2 selects the additive mixing of these two frequencies, and delivers a 20-MHz to 19-MHz signal that is successively amplified by A3, divided by 10 in divider D3 and filtered by band-pass filter FL3.

. The output frequency of each Standard Decade includes therefore the ten frequency increments generated by this Decade, together with the frequency increments elaborated in the preceding subassemblies of the iterative synthesis chain.

The selection of an Interpolation range higher than the weight of the frequency increments elaborated in the Standard Decade entails the inhibition of this Decade by switching off its + 6 V supply voltage. Besides, in the Standard Decade generating frequency increments whose weight is equal to one

tenth the Interpolation range, the synthesized frequency is replaced at filter FL3 by frequency F12 :
2.1 MHz/1.9 MHz coming from option 3114B (see section VI-11).

For instance, selecting a $\pm$ 1 kHz Interpolation range causes the inhibition of the first three Standard Decades, while frequency F12 is substituted for the synthesized frequency in the third Standard Decade.

PRINCIPLE OF PROGRAMMABLE COUNTER DP2
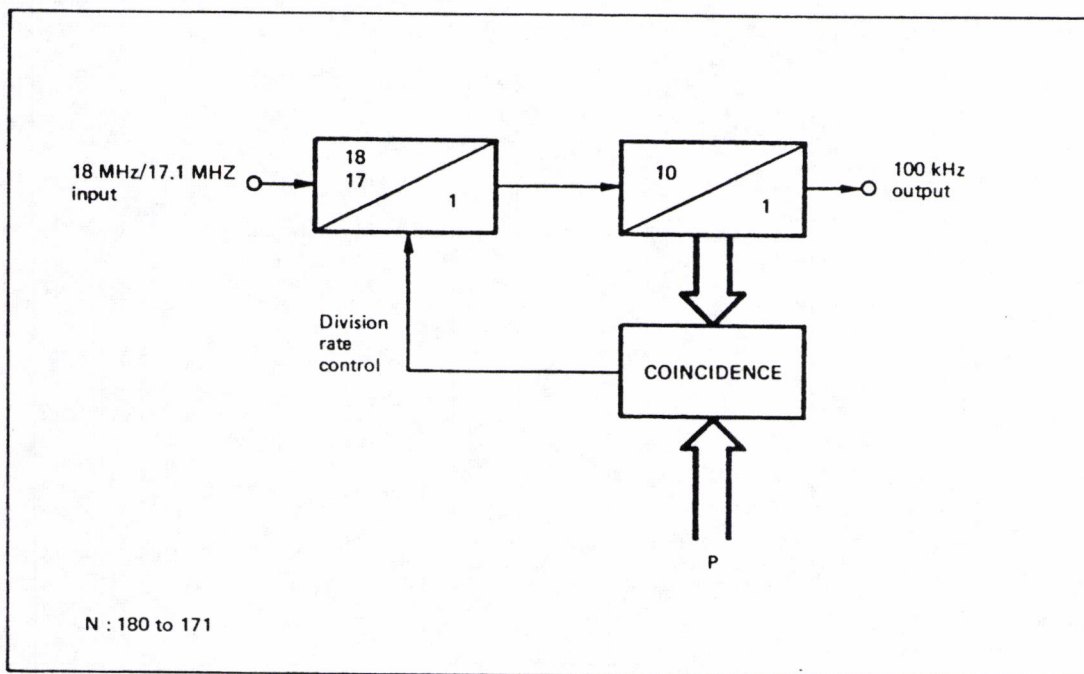
Figure VI-6 PRINCIPLE OF COUNTER DP2

The programmable counter DP2 consists essentially of a divider by 17 or 18, a divider by 10 and a coincidence circuit comparing the state of the divider by 10 with the value P : 0 to 9 of the BCD programming signals.

During each counting cycle, this coincidence circuit makes the division rate of the front divider P times equal to 17 and 10-P times equal to 18. The overall division rate N may thus be written :

$$N = 17 \, P + 18 \, (10 - P).$$

The divider by 10 consists of a 74 LS 90 decade counter (integrated circuit SN9, plate VI-4).

The coincidence circuit is made of three NAND gates (integrated circuit SN10) decoding the various states of the divider by 10 according to the table of figure VI-7, and of four NOR gates detecting the coincidence between the programming signals and the divider states decoded by the NAND gates.

For instance, if a "0" logic level is applied to code inputs $\overline{1}$ - $\overline{2}$ - $\overline{4}$ and if a "1" logic level is applied to code input $\overline{8}$, the coincidence circuit detects states 2-3, 4-5-6-7 and 9 of the divider by 10. The front divider divides therefore 7 times by 17 and 3 times by 18 during each counting cycle, which gives N = 173 as overall division rate.

The front divider consists of a divider by 8 (integrated circuits SN5 and SN7, plate VI-4) preceded with a divider by 2, 3 or 4 (integrated circuits SN5 and SN6) whose division rate is controlled by two NOR gates (integrated circuit SN8).

Divider States	A	B	C	D	Decoding
0	0	0	0	0	
1	1	0	0	0	
2	0	1	0	0	$\overline{2}$
3	1	1	0	0	
4	0	0	1	0	$\overline{8}$
5	1	0	1	0	$\overline{4}$
6	0	1	1	0	
7	1	1	1	0	
8	0	0	0	1	
9	1	0	0	1	$\overline{1}$
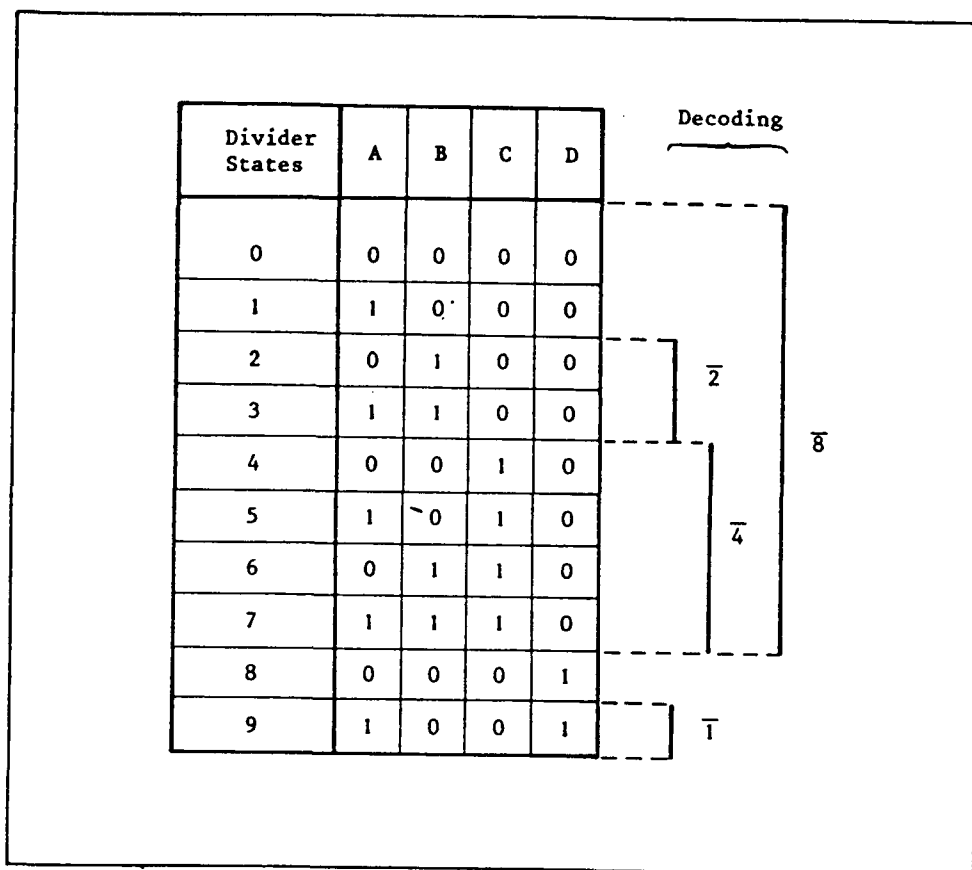
Figure VI-7   DECODING OF DIVIDER BY 10

Depending whether the front divider must divide by 17 or by 18, this division rate is respectively equal to 3 or 4 one time per cycle of the front divider, and equal to 2 the rest of the time.

VI-4   TWENTY-INCREMENT UNIT

See block diagram on plate VI-1 and figure VI-8, as well as schematic on plate VI-5.

This subassembly elaborates the 10^4 Hz and 10^5 Hz increments of the output frequency, while incorporating the 10^{-2} Hz to 10^3 Hz increments carried by frequency F5 : 2.1 MHz/1.9 MHz issued from the fourth Standard Decade.

The elaboration of the 10^4 Hz and 10^5 Hz increments is achieved by means of a phase-locked loop including oscillator 03, programmable counter DP3 and phase/frequency comparator CP3. Oscillator 03 delivers a 6.44 MHz to 7.2 MHz frequency that programmable counter DP3 divides by N, respectively comprised between 180 and 161. The frequency issued from this DP3 counter is then compared in phase/frequency comparator CP3 with a 40 kHz reference obtained by dividing by 5 frequency F10 : 200 kHz issued from the Time Base. Comparator CP3 thus provides a DC voltage phase-locking oscillator 03 to a frequency equal to N times the 40 kHz reference.

The collection of the 10^{-2} Hz to 10^3 Hz increments carried by frequency F5 and the 10^4 Hz and 10^5 Hz increments of the output frequency is achieved through a second phase-locked loop including oscillator O4, mixer M2, filter FL5, amplifier A6, divider D7 and phase/frequency comparator CP4.

Figure VI-8 TWENTY-INCREMENT UNIT

Oscillator O4 delivers a frequency variable from 8 MHz to 7.2 MHz that mixer M2 mixes with the 7.2 MHz to 6.44 MHz frequency generated by oscillator O3 and filtered by band-pass filter FL4. The substractive beat of these two frequencies is selected by the band-pass filter FL5, thus delivering a 840 kHz to 760 kHz frequency. After amplification by A6 and division by 2 in divider D7, this frequency is applied to phase/frequency comparator CP4, where it is compared with the frequency variable from 420 kHz to 380 kHz obtained by dividing by 5 in divider D6 frequency F5 : 2.1 MHz/1.9 MHz issued from the fourth Standard Decade. Thus, comparator CP4 provides a DC voltage which, by means of the approach voltage issued from comparator CP3, phase-locks oscillator O4 to a frequency comprising both the increments generated by oscillator O3 and the increments elaborated in the Centade and the Standard Decades.

Programmable counter DP3 consists of two 74 163 binary dividers (integrated circuits SN2 and SN3, figure VI-9 and plate VI-5) whose certain output states are detected by four NAND gates (integrated circuit SN5) controlling the parallel loading of the programming signals.
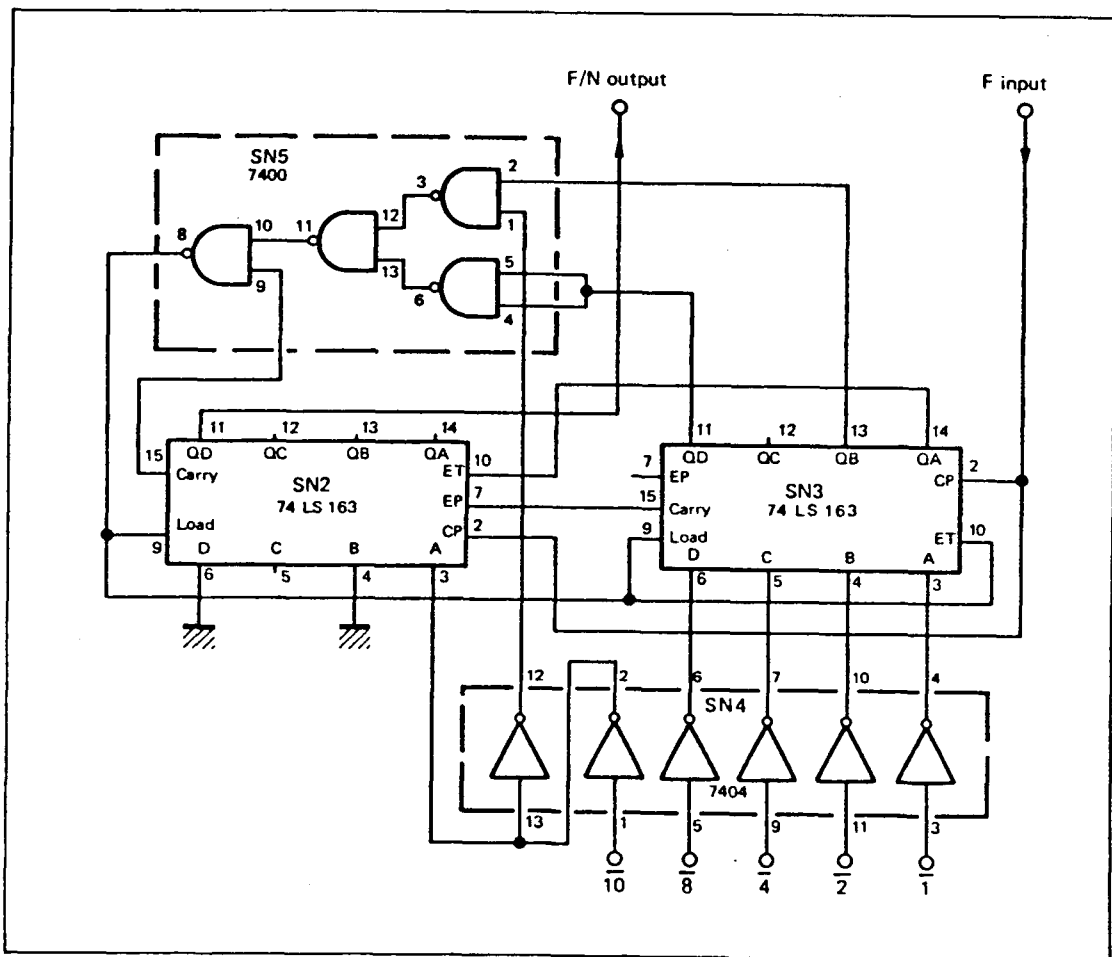

Figure VI-9 PRINCIPLE OF COUNTER DP3

The presence of two dividers by 16 provides 16^2 = 256 different logic states, in which N : 180 to 161 are actually used during each counting cycle. These N logic states correspond to the difference between the state detected by the NAND gates of integrated circuit SN5 and the value of the parallel loading of the two dividers by 16.

The parallel loading is achieved after a "0" logic level has appeared on the "Load" input of the two dividers, which requires both that SN2 has reached the 1111 state and that the Qa, Qb, and Qd outputs of SN3 satisfy the following equation, in which X is the $\overline{10}$ programming signal of counter DP3 :

$$Qa \ (X.Qb \ + \ Qd) = 1$$

Two cases can then be considered depending on whether X = 1, corresponding to an N division rate comprised between 180 and 171, or X = 0 corresponding to N comprised between 170 and 161.

a) X = 1

In this case, the "0" level appears on the "Load" inputs when SN2 reaches the 1111 state and SN3 the 0011 state, which corresponds to the state (15 x 16) + 3 = 243 of counter DP2.

The parallel loading which occurs at the clock pulse following the appearance of the "0" level on the "Load" inputs makes SN2 return to the 0100 state, whilst SN3 is loaded at the value P : 0 to 9 programmed by the four $\overline{1} - \overline{2} - \overline{4} - \overline{8}$ coding signals. This parallel loading of the two dividers corresponds to the state (4 x 16) + P = 64 + P of counter DP2.

As the N division rate is equal to the number of states comprises between the 243 final state and the 64 + P initial state of the counter, the result is : N = 180 - P.

b) X = 0

In this case, the "0" level appears on the "Load" inputs when SN2 reaches the 1111 state and SN3 the 1011 state, which corresponds to the (15 x 16) + 9 = 249 state of counter DP2.

The parallel loading which occurs at the clock pulse following the appearance of the "0" level on the "Load" inputs makes SN2 return to the 0101 state, whilst SN3 is loaded at the value P : 0 to 9 programmed by the four $\overline{1} - \overline{2} - \overline{4} - \overline{8}$ coding signals. This parallel loading of the two dividers corresponds to the (5 x 16) + P = 80 + P state of counter DP2.

The N division rate, equal to the number of states comprised between the 249 final state and the 80 + P initial state, becomes in this case : N = 170 - P.

VI-5 OUTPUT MIXER

See block diagram on plate VI-1 and figure VI-10, as well as schematic on plate VI-6.
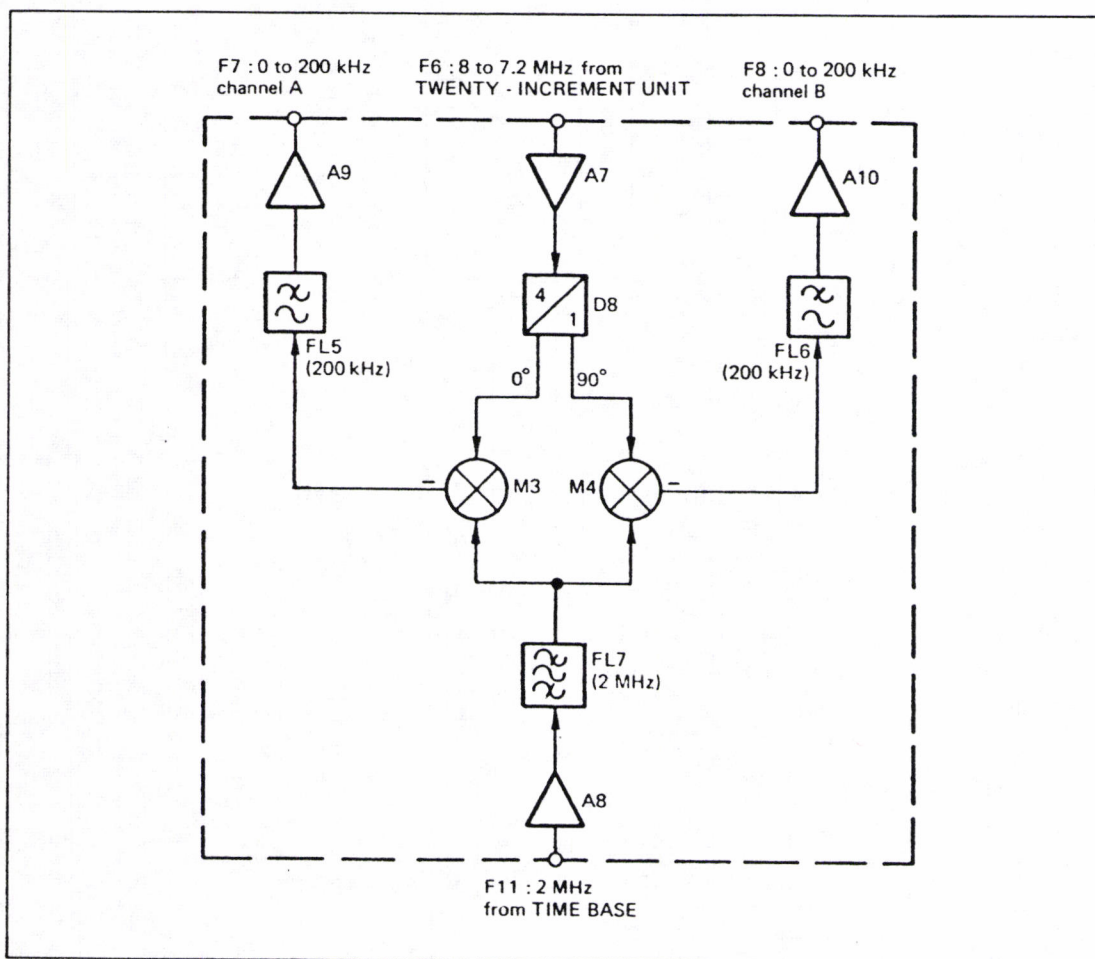

Figure VI-10 OUTPUT MIXER

This subassembly delivers the output frequency of the synthesizer in the form of two signals in phase quadrature.

Frequency F6 : 8 MHz/7.2 MHz issued from the Twenty-Increment unit is amplified by A7, then divided by 4 in Johnson counter D8, which provides two signals phase-shifted by 90° with a 2 MHz to 1.8 MHz frequency.

Two mixers M3 and M4 mix these signals with frequency F11 : 2 MHz issued from the Time Base, this frequency being pre-amplified by A8 and filtered by band-pass filter FL7.

The selection by low-pass filter FL5 of the substractive beat between the signals sent to mixer M3 provides the F7 output frequency of channel A of the synthesizer. After amplification by A9, this frequency is directed both towards the Function Switch, connector (J3) on the rear panel of the instrument and, where applicable, towards option 3112B.

In the same way, low-pass filter FL6 selects the substractive beat between the signals sent to mixer M4 and delivers the F8 output frequency of channel B of the synthesizer. After amplification by A10, this frequency is directed both towards the Function Switch, connector (J4) and, where applicable, towards option 3112B.

VI-6 FUNCTION SWITCH

The waveform and the amplitude of the generator synthesizer output signals are determined by the Function Switch, whose schematic is on plate VI-9.

The F7 sine wave issued from the Output Mixer is, depending on the (K6) keyboard command, changed into positive, symmetrical or negative square waves through hysteresis comparators SN1 and SN2, or transmitted in its original form to the Output Amplifier. In both cases, depending on the position of key (K7), a resistor bridge and potentiometer (P1) provide a calibrated or continuously variable output level to main output A.

The F8 sine wave issued from the Output Mixer is always transmitted by the Function Switch without change of waveform. Depending on the position of key (K3), a resistor bridge and potentiometer (P2) provide a calibrated or continuously variable output level to main output B.

VI-7 OUTPUT AMPLIFIER

The Output Amplifier, the electrical diagram of which is on plate VI-7, provides 10 Vpeak e.m.f. to the signals issued from the Function Switch. This amplification is performed on channels A and B respectively through two identical amplifiers A11 and A12, each comprising three stages with complementary transistors.

VI-8 TIME BASE

See block diagram on plate VI-1 and figure VI-11, as well as schematic on plate VI-8.

The elaboration of the synthesizer output frequency is achieved from a 10 MHz reference, successively divided by 5 in divider D9 and by 10 in divider D10. These two dividers respectively deliver frequency F11 : 2 MHz aimed at the Output Mixer and frequency aimed at the Twenty-Increment unit.

When switch (K10) is on the "Internal" position, this 10 MHz reference, available on connector (J5) at an approximate level of 100 mVrms/50 Ω, is generated by crystal oscillator 05.

When switch (K10) is on the "External" position, crystal oscillator 05 is inhibited and the frequency synthesis is achieved from an external reference applied to connector (J5).
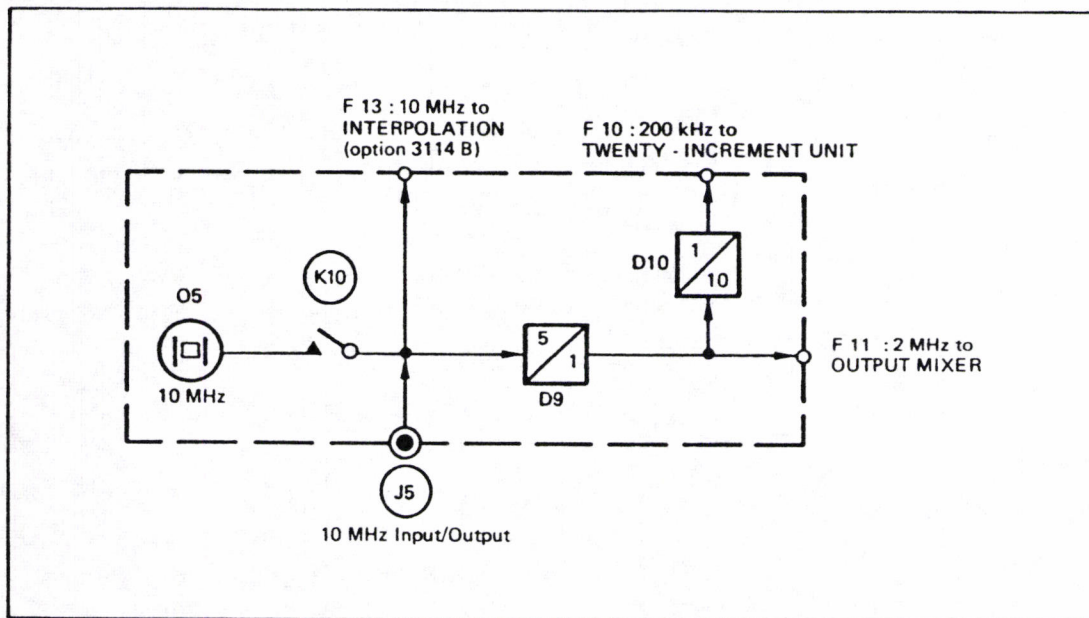

Figure VI-11   TIME BASE

VI-9 PROGRAMMABLE ATTENUATOR OPTION 3111B

See block diagram on plate VI-2 and schematics on plates VI-13, VI-14 and VI-15.

The programmable attenuator includes ten π cells having the following values : 0.1 dB - 0.2 dB - 0.4 dB - 0.8 dB - 1.6 dB - 3.2 dB - 6.4 dB - 10 dB - 20 dB - 40 dB.

The 10 dB steps of the attenuation are provided by the 10 dB, 20 dB and 40 dB cells, directly controlled in parallel BCD code.

The 0.1 dB and 1 dB steps of the attenuation are achieved through the 0.1 dB to 6.4 dB cells. These cells are controlled in binary code by two 4008 adders (integrated circuits SN1 and SN2, plate VI-13) performing the BCD/Binary transcoding.

For example, a 14.9 dB attenuation is obtained by validating the 10 dB cell as well as the 3.2 dB, 1.6 dB and 0.1 dB cells.

The parallel BCD signals programming the attenuation come either from the Switch Decoding circuit (plate VI-14) in Local mode, or from the Code Filter (plate VI-15) in Remote mode.

See block diagram on plate VI-2 and figure VI-12, as well as schematics on plates VI-15, VI-16, VI-17 and VI-18.
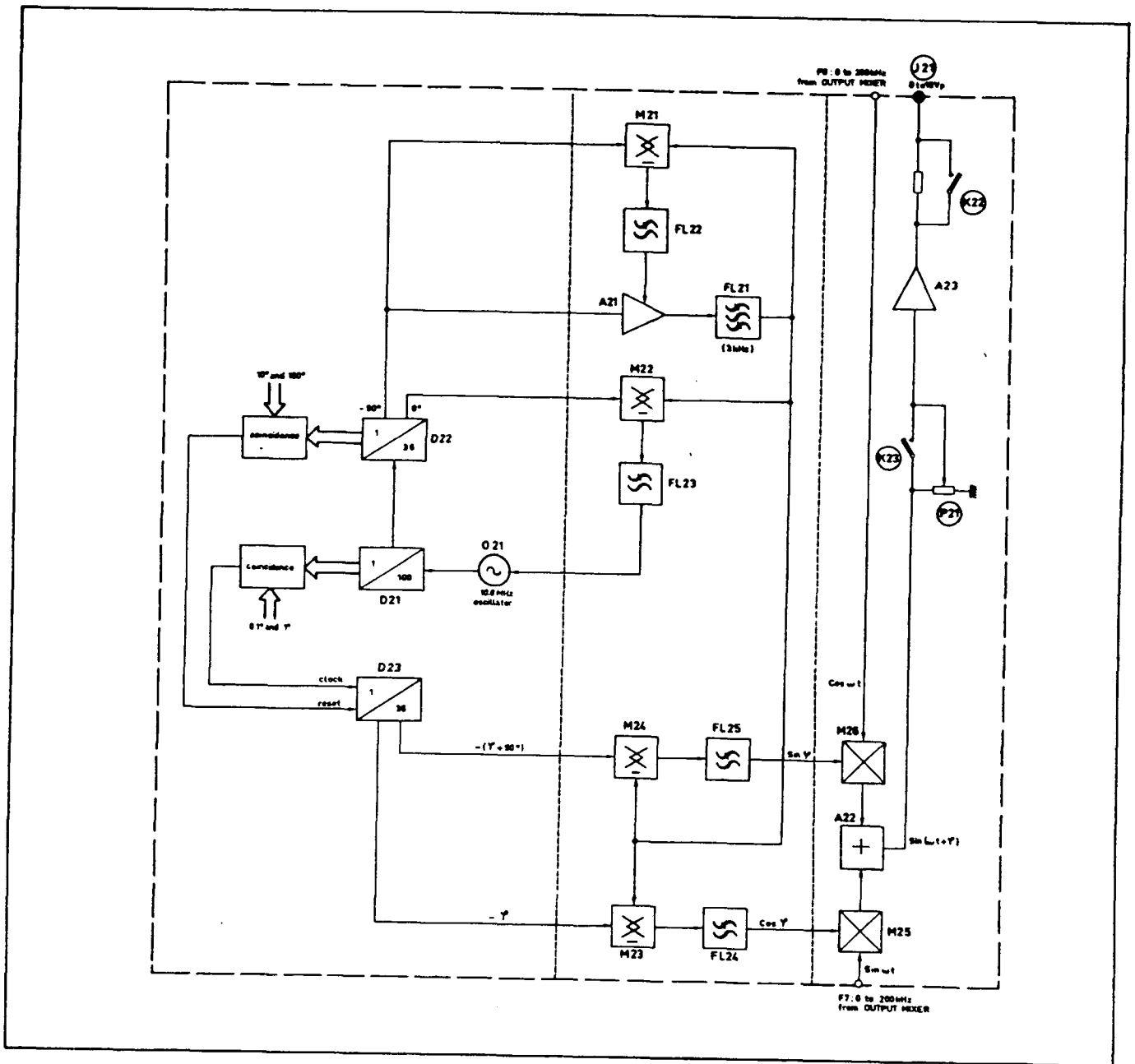

Figure VI-12 PROGRAMMABLE PHASE-SHIFTER OPTION 3112B

The elaboration of the phase-shifted signal is achieved by multiplying the signals issued from channels A and B of the Output Mixer by two DC voltages representing respectively the cosine and the sine of the ϕ phase-shift angle, then by adding the signals obtained. This elaboration process of the phase-shifted signal corresponds to the mathematical formula :

$$\sin (\omega t + \phi) = \cos \phi . \sin \omega t + \sin \phi . \cos \omega t$$

The DC voltages representing $\cos \phi$ are generated from three 3 kHz signals, respectively phase-shifted from $- 90°$, $- \phi$ and $- (90° + \phi)$ with regard to a reference signal. These signals are obtained by dividing a 10.8 MHz frequency by 3600 through a counter by 100, two counters by 36 and two coincidence circuits allowing the ϕ phase-shift programming.

This subassembly, whose schematic is on plate VI-16, generates the digital signals from which the DC voltages representing cos ϕ and sin ϕ are elaborated.

The 10.8 MHz frequency that oscillator 021 generates is divided by 100 in counter D21 consisting of two 74 162 decades (integrated circuits SN2 and SN3, plate VI-16). The 108 kHz frequency issued from counter D21 is divided by 36 in counter D22, which provides both BCD signals permitting the 10° and 100° steps programming of the ϕ phase-shift and four 3 kHz signals in phase quadrature.

The BCD signals are provided by a divider by 36, consisting of two 74 162 decades (integrated circuits SN4 and SN5) whose synchronous reset is ensured by a NAND gate (integrated circuit SN13) detecting the state 35 of the divider. The signals in phase-quadrature are generated by a Johnson counter consisting of two J-K flip-flops (integrated circuits SN15 and SN16) which change state at the same rate as the divider by 36, so as to deliver 3 kHz frequency signals.

Counter D21 also provides BCD signals which are applied to a coincidence circuit receiving the programming signals of the 0.1° and 1° steps of the ϕ phase-shift. This coincidence circuit, made up of exclusive-OR gates (integrated circuits SN6 and SN7) whose outputs are linked together so as to constitute a wired AND, transmits to counter D23 a 108 kHz frequency delayed by the number of clock pulses equal to the programmed value of the 0.1° and 1° steps. Counter D23, which consists of two dividers by 3 (integrated circuits SN8 and SN9) followed by a Johnson counter (integrated circuit SN10), divides this frequency by 36 and delivers four 3 kHz signals in phase quadrature. A second exclusive-OR coincidence circuit (integrated circuits SN11, SN12 and SN14) receiving the BCD signals issued from counter D22 and the programming signals of the 10° and 100° steps of the ϕ phase-shift, controls the reset of this D23 counter, so that its output signals are phase-shifted from ϕ with regard to the signals delivered by counter D22.

VI-10-2 GENERATION sin ϕ / cos ϕ

This subassembly, whose schematic is on plate VI-17, elaborates the DC voltages representing the cosine and the sine of the ϕ phase-shift angle.

The signal phase-shifted from - 90° that counter D22 delivers is made sinusoidal by band-pass filter FL21 preceded with amplifier A21. The gain of this amplifier is regulated through a synchronous detection performed by mixer M21 followed by low-pass filter FL22, which provides a constant level to the sine wave delivered by filter FL21.

On the other hand, mixer M22 followed by low-pass filter FL23 achieves a phase detection between this sinusoidal signal and the 0° reference signal delivered by counter D22. Thus, low-pass filter FL23 provides a DC voltage phase-locking oscillator 021 to the frequency for which band-pass filter FL21 brings no phase-shift.

Mixer M23 performs the frequency beat between the sine wave delivered by filter FL21 and the signal phase-shifted by -ϕ issued from counter D23, which provides at the output of low-pass filter FL24 a DC voltage representing cos ϕ.

In the same way, mixer M24 performs the frequency beat between the sine wave delivered by filter FL21 and the signal phase-shifted by - (90° + ϕ) issued from counter D23, so as to obtain at the output of low-pass filter FL25 a DC voltage representing sin ϕ.

This subassembly, whose schematic is on plate VI-18, delivers the sin ($\omega t + \phi$) output signal by multiplying the sine waves issued from channels A and B of the Output Mixer by the two DC voltages generated in the preceding subassembly. Linear multiplier M25 realizes the product between the voltage representing cos ϕ and the F7 signal issued from the Output Mixer, whilst the product between the voltage representing sin ϕ and the F8 signal issued from the Output Mixer is carried out by linear multiplier M26.

The cos ϕ. sin ωt and sin ϕ. cos ωt signals respectively delivered by M25 and M26 are summed up in current adder A22, which thereby provides a sine wave phase-shifted from ϕ with regard to the signal of channel A of the synthesizer. The level of this phase-shifted signal is adjusted by potentiometer (P21) or calibrated by a resistor bridge, then amplified by A23 which delivers to output connector (J21) up to 10 Vpeak electromotive force.

VI-11 SEARCH AND SWEEP OPTION 3114B

See block diagram on plate VI-2 and figure VI-13, as well as schematics on plates VI-19 and VI-20.
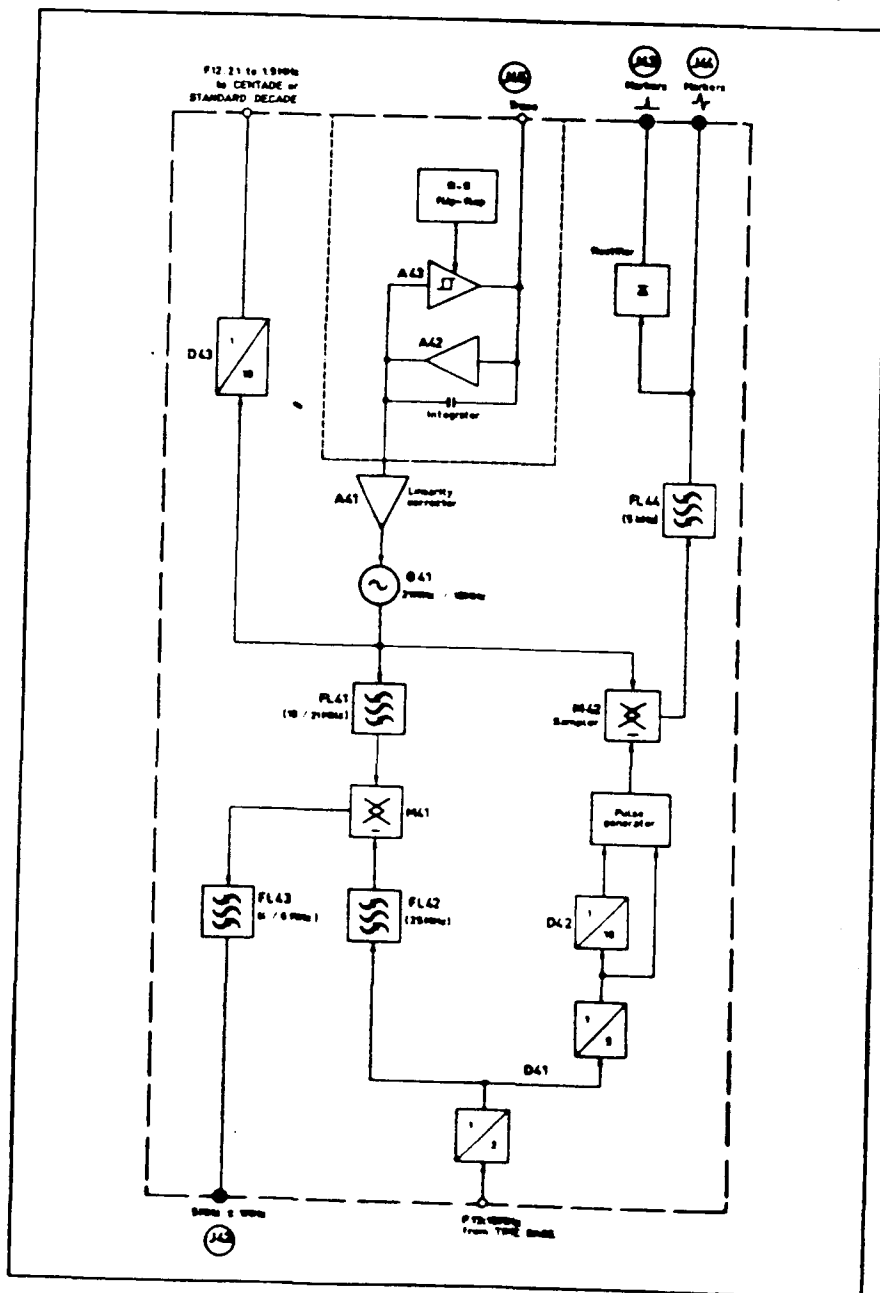

Figure VI-13 SEARCH AND SWEEP OPTION 3114B

The Search and Sweep option delivers frequency F12 : 2.1 MHz/1.9 MHz which, substituted for one of the F1 to F5 frequencies synthesized by the Centade and the Standard Decades, provides a continuous variation of the synthesizer output frequency. Moreover, twenty-one markers obtained by beat between th frequency generated by the interpolation oscillator and a 100 kHz frequency directly derived from refer ence frequency F13 : 10 MHz issued from the Time Base, allow use of the 3100B + 3114B unit as a sweeper

VI-11-1 SWEEP

This subassembly, whose schematic is on plate VI-19, delivers the signal controlling the frequenc of interpolation oscillator 041 according to the operating mode selected on keyboard (K41).

- In Search mode, the frequency of oscillator 041 is adjusted through potentiometer (P41).

- In External mode, this frequency is controlled by the voltage applied to connector (J41), pos- sibly attenuated by potentiometer (P42).

- In Free-run mode, hysteresis comparator A43 and integrator A42 deliver symmetrical triangles ensuring the sweeping of oscillator 041. The duration of these triangles is determined through a resisto network switched by (K45) so as to fix the sweep duration between 10 ms and 300 s. The amplitude control of these triangles achieved by potentiometer (P42) allows adjustment of the sweep width, while the super- position of a DC voltage determined by potentiometer (P41) provides continuous adjustment of the center frequency around which the sweep is achieved.

- In Triggered mode, the frequency of oscillator 041 is swept by a sawtooth generated through hysteresis comparator A43 and integrator A42, changed into a one-shot circuit by the R-S flip-flop. This flip-flop delivers at the end of each sawtooth a "0" logic level which brings the hysteresis comparator back to its original state. Pressing "Stop" key (K43) or applying a "0" level to socket (J47) also cause the appearance of this "0" level on the R-S flip-flop, which will not disappear until "Start" key (K42) is pressed or until a "0" level is applied to socket (J46). As in free-run mode, the sweep duration is determined by switch (K45), the sweep width is adjusted by potentiometer (P42), whilst potentiometer (P41) provides continuous adjustment of the center frequency.

VI-11-2 INTERPOLATION

This subassembly, whose schematic is on plate VI-20, delivers frequency F12 : 2.1 MHz/1.9 MHz as well as the markers and the 5 MHz ± 1 MHz frequency representing the output frequency variation of the generator synthesizer.

Oscillator 041 generates a frequency variable from 21 MHz to 19 MHz, from which frequency F12: 2.1 MHz/1.9 MHz is directly derived through a division by 10 in divider D43 . This oscillator is con- trolled through linearity corrector A41 by the control voltage delivered by the Sweep subassembly.

Mixer M4 and band-pass filter FL43 make a substractive beat between the frequency of oscillator 04 previously filtered by band-pass filter FL41, and a 25 MHz frequency delivered by band-pass filter FL42. As this 25 MHz frequency is directly derived from frequency F13 : 10 MHz through division by 2 and har- monic selection, the substractive beat selected by filter FL43 provides a 5 MHz ± 1 MHz frequency whose variation represents exactly the variation of the synthesizer output frequency.

Reference frequency F13 : 10 MHz issued from the Time Base is divided by 100 in dividers D41 and D42, the outputs of which are linked to a NAND gate pulse generator delivering both 100 kHz frequency pulses and 1 MHz frequency pulses having an amplitude double that of the first ones. These pulses are applied to sampler M42, receiving on the other hand, the 21 MHz/19 MHz frequency generated by

oscillator 041. Low-pass filter FL44 selects the 21 coincidences between the frequency of oscillator 041 and the sampling pulses, which provides 3 markers indicating the center and the ends of the dispersion range as well as 18 intermediate markers. The markers issued from low-pass filter FL44 are directly available on connector (J44) whilst connector (J43) delivers amplified and rectified markers.

OPTION IEEE BUS OPERATING INSTRUCTIONS

This option made of two boards translates the IEEE bus information into parallel BCD signals. It substitutes in programming to the local synthesizer controls.

The board connecteur isolate the IEEE bus signals from those of the instrument.

The board bus carries the exchange protocol of the IEEE bus, the address recognition, the Local/Remote control and the five registers decoding. Four of them, namely A, B, C and D are used by the wired options of the instrument (3111 and 3112), and the fifth register is reserved to the frequency programmation.

Both option 3111 and 3112 can be programmed by either registers A, B, C or D. *

The frequency is programmed by hundredths of a Hz steps.
The phase shift is programmed by tens of a degree steps.
The attenuation is programmed in tens of a dB steps.

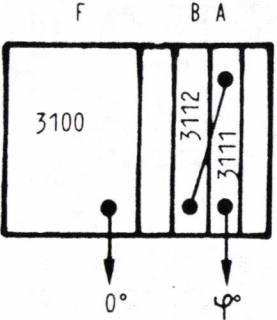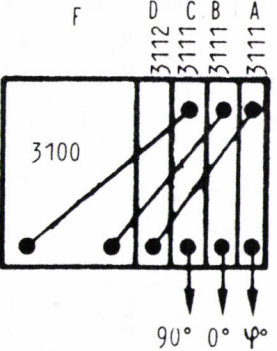The message is enabled by a carriage return (RC) a question mark (?) or a end of message trigger.

Functions : AH1, TØ, SHØ, LEØ, SRØ, RL2, TEØ, L1, PPØ, DC1, DT1, CØ.
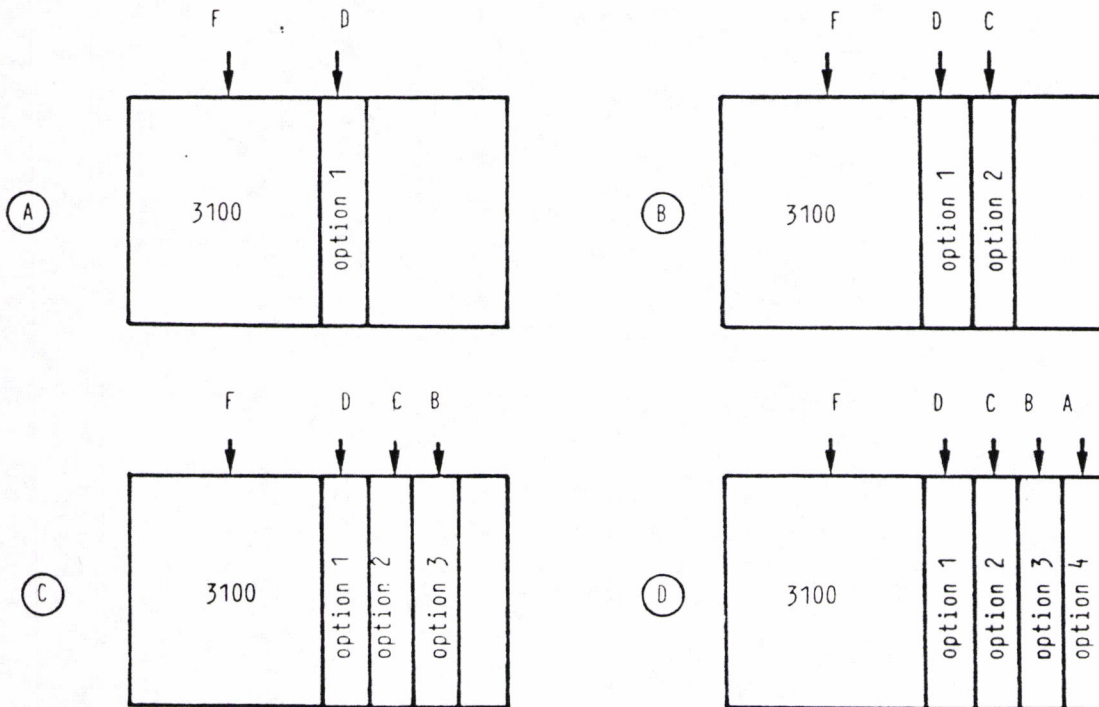
* Definition of the programming prefix corresponding to the wired option.

IEEE BUS OPTION BLOCK DIAGRAM

ATN
IFC
NDAC
NRFD
DAV
REN

ISOLATOR

HEF 4738

LOCAL/
REMOTE

DI01
à DI07

DI01 à DI07

DECODING

REGISTER F	REGISTER D	REGISTER C	REGISTER B	REGISTER A

MEMORY F	MEMORY D	MEMORY C	MEMORY B	MEMORY A

10^0 à 10^7 10^0 à 10^3 10^0 à 10^3 10^0 à 10^3 10^0 à 10^3

		HP 85 address Ø	HP 9825 address Ø	PET address 4
	a) phase sweep	1Ø OUTPUT 7ØØ; "F1ØØØØØAØ 2Ø FOR X = Ø to 35ØØ STEP 1Ø 3Ø OUTPUT 7ØØ; "B", X 4Ø NEXT X 5Ø GOTO 2Ø	Ø wrt 7ØØ. "F1ØØØØØAØ" 1 for X = Ø to 35ØØ by 1Ø 2 wrt 7ØØ. "B". X 3 next X 4 gto 1	1Ø OPEN 1,4 2Ø PRINT # 1. "F1ØØØØØAØ" 3Ø FOR X = Ø to 35ØØ STEP 1Ø 4Ø PRINT # 1. "B". X 5Ø NEXT X 6Ø GOTO 3Ø
	b) level sweep	1Ø OUTPUT 7ØØ;"F1ØØØØØB1ØØ" 2Ø FOR X = Ø to 5ØØ STEP 1Ø 3Ø OUTPUT 7ØØ; "A", X 4Ø NEXT X 5Ø GOTO 2Ø	Ø wrt 7ØØ. "F1ØØØØØB1ØØ" 1 for X = Ø to 5ØØ by 1Ø 2 wrt 7ØØ. "A", X 3 next X 4 gto 1	1Ø OPEN 1,4 2Ø PRINT # 1. "F1ØØØØØB1ØØ" 3Ø FOR X = Ø to 5ØØ STEP 1Ø 4Ø PRINT # . "A". X 5Ø NEXT X 6Ø GOTO 3Ø

	c) frequency sweep	1Ø DISP "Start frequency"
		  @INPUT F
		2Ø DISP "Stop frequency"
		  @INPUT X
		3Ø OUTPUT 7ØØ ; "AØ"
		4Ø FOR J = F to X STEP 1Ø
		5Ø OUTPUT 7ØØ ; "F", J
		6Ø NEXT J
		7Ø GOTO 1Ø
			Ø ent"Start frequency", F
			1 ent"Stop frequency". X
			2 wrt 7ØØ. "AØ"
			3 for J = F to X by 1Ø
			4 wrt 7ØØ, "F". J
			5 next J
			6 gto Ø
				1Ø OPEN 1,4
				2Ø PRINT"Start frequency" :
				  INPUT F
				3Ø PRINT"Stop frequency":INPUT X
				4Ø PRINT # 1. "AØ"
				5Ø FOR J = F to X STEP 1Ø
				6Ø PRINT # 1, "F". J
				7Ø NEXT J
				8Ø GOTO 2Ø

	d) phase than level sweep	1Ø DISP"Fréquency"@INPUT F
		2Ø OUTPUT 7ØØ; "AØF", F
		3Ø FOR X = Ø to 35ØØ STEP 1Ø
		4Ø OUTPUT 7ØØ ; "D", X
		5Ø NEXT X
		6Ø FOR X = Ø to 5ØØ STEP 1Ø
		7Ø OUTPUT 7ØØ;"A", X. "B".
		  X. "C", X
		8Ø NEXT X
		
		9Ø GOTO 1Ø
			Ø ent"Fréquency". F
			1 wrt 7ØØ. "AØF", F
			2 for X = Ø to 35ØØ by 1Ø
			3 wrt 7ØØ. "D". X
			4 next X
			5 for X = Ø to 5ØØ by 1Ø
			6 wrt 7ØØ. "A". X. "B". X.
			  "C". X
			7 next X
			8 gto Ø
				1Ø OPEN 1,4
				2Ø PRINT"Fréquency":INPUT F
				3Ø PRINT # 1. "AØF". F
				4Ø FOR X = Ø to 35ØØ STEP 1Ø
				5Ø PRINT # 1. "D". X
				6Ø NEXT X
				7Ø FOR X = Ø to 5ØØ STEP 1Ø
				8Ø PRINT # 1. "A". X. "B". X.
				  "C". X
				9Ø NEXT X
				1ØØ GOTO 2Ø

PET 2001

* Equipment address : 5

```
1∅          OPEN # 1,5
2∅          PRINT "HIGH FREQ LIMIT"
3∅          INPUT F1
4∅          PRINT "LOW FREQ LIMIT"
5∅          INPUT F2
6∅          PRINT "FREQUENCY STEP"
7∅          INPUT F3
8∅          PRINT "GOING UP LEVEL"
9∅          INPUT A1
1∅∅         PRINT "GOING DOWN LEVEL"
11∅         INPUT A2
12∅         PRINT "TIME"
13∅         INPUT T
14∅         FOR F = F1 TO T2 STEP-F3
15∅         PRINT # 1, "F", F, "A", A2
16∅         FOR I = 1 TO T : NEXT I
17∅         NEXT F
18∅         FOR F = F2 TO F1 STEP F3
19∅         PRINT # 1, "F", F, "A", A1
2∅∅         FOR I = 1 TO F : NEXT I
21∅         NEXT F
22∅         GOTO 2∅
```